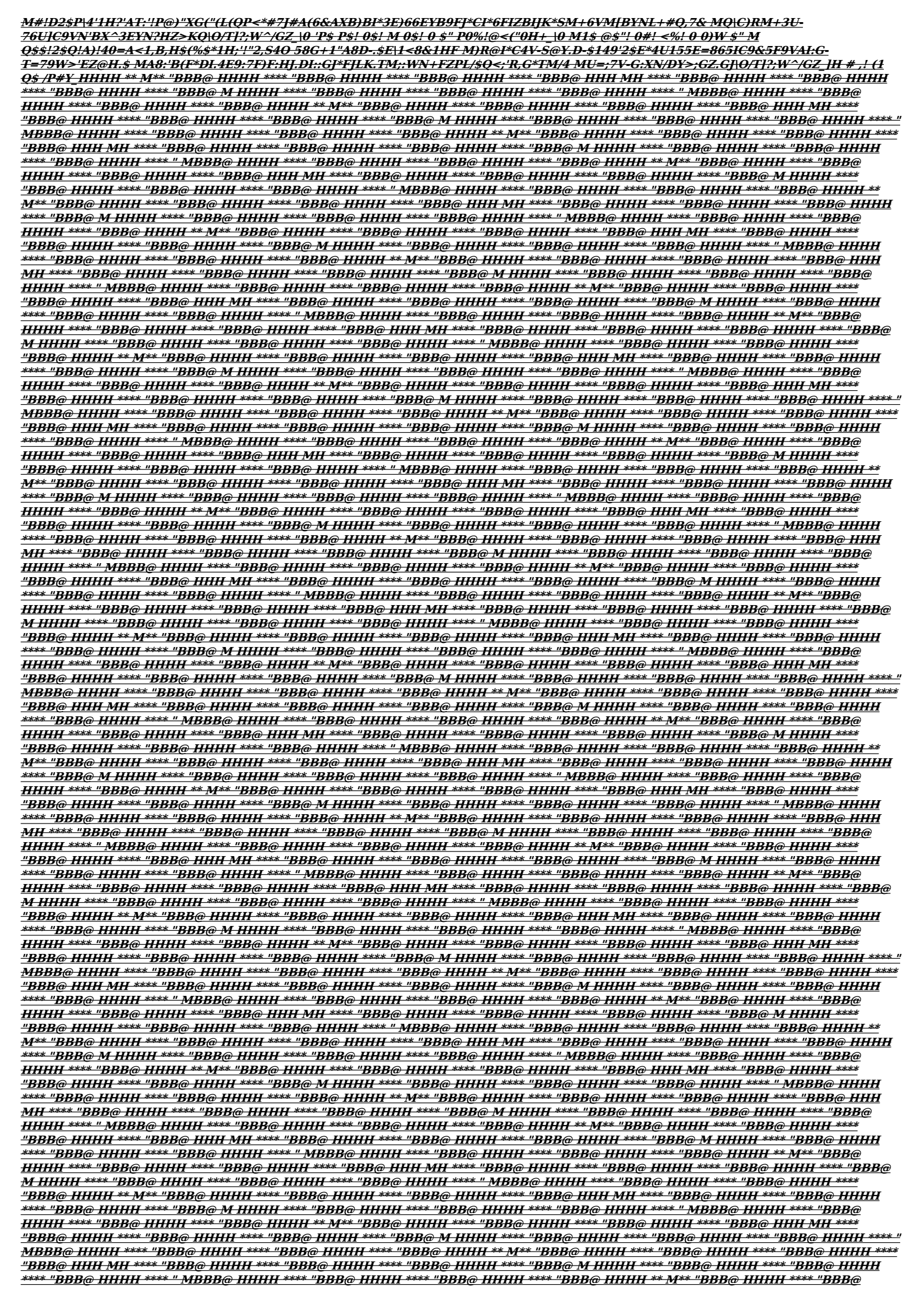

0000937966-24-0000266-K ASML HOLDING NV 20241118202411180604180604180604180 0000937966-24-000026 6-K 229 20241118 20241118 20241118 ASML HOLDING NV 0000937966 3559 000000000 1231 6-K 34 001-33463 241469646 DE RUN 6501 DR VELDHOVEN P7 5504 31402683000 P.O. BOX 324 AH VELDHOVEN P7 5500 ASM LITHOGRAPHY HOLDING NV 19950215 6-K 1 form6-kinvestordaypresenta.htm 6-K DocumentSECURITIES AND EXCHANGE COMMISSIONWashington, D.C. 20549 ______________________FORM 6-KREPORT OF FOREIGN PRIVATE ISSUERPURSUANT TO RULE 13a-16 OR 15d-16OF THE SECURITIES EXCHANGE ACT OF 1934For November 18, 2024Commission File Number 001-33463______________________ASML Holding N.V.De Run 65015504 DR VeldhovenThe Netherlands(Address of principal executive offices)______________________Indicate by check mark whether the registrant files or will file annual reports under cover of Form 20-F or Form 40-F.Form 20-F x Form 40-F Â¨Indicate by check mark if the registrant is submitting the Form 6-K on paper as permitted by Regulation S-T Rule 101(b)(1): Â¨Indicate by check mark if the registrant is submitting the Form 6-K on paper as permitted by Regulation S-T Rule 101(b)(7): Â¨EXHIBITS TO THIS REPORT ON FORM 6-K ARE INCORPORATED BY REFERENCE IN THE REGISTRATION STATEMENT ON FORM S-8 (FILE NO. 333-116337), THE REGISTRATION STATEMENT ON FORM S-8 (FILE NO. 333-126340), THE REGISTRATION STATEMENT ON FORM S-8 (FILE NO. 333-136362), THE REGISTRATION STATEMENT ON FORM S-8 (FILE NO. 333-141125), THE REGISTRATION STATEMENT ON FORM S-8 (FILE NO. 333-142254), THE REGISTRATION STATEMENT ON FORM S-8 (FILE NO. 333-144356), THE REGISTRATION STATEMENT ON FORM S-8 (FILE NO. 333-147128), THE REGISTRATION STATEMENT ON FORM S-8 (FILE NO. 333-153277), THE REGISTRATION STATEMENT ON FORM S-8 (FILE NO. 333-162439), THE REGISTRATION STATEMENT ON FORM S-8 (FILE NO. 333-170034), THE REGISTRATION STATEMENT ON FORM S-8 (FILE NO. 333-188938), THE REGISTRATION STATEMENT ON FORM S-8 (FILE NO. 333-190023), THE REGISTRATION STATEMENT ON FORM S-8 (FILE NO. 333-192951), THE REGISTRATION STATEMENT ON FORM S-8 (FILE NO. 333-203390), THE REGISTRATION STATEMENT ON FORM S-8 (FILE NO. 333-219442) AND THE REGISTRATION STATEMENT ON FORM S-8 (FILE NO. 333-227464) OF ASML HOLDING N.V. AND IN THE OUTSTANDING PROSPECTUSES CONTAINED IN SUCH REGISTRATION STATEMENTS.ExhibitsÂ 99.1Â Â Â Â â€œOpening remarks", presentation dated November 14, 202499.2Â Â Â Â â€œGlobal market trends, Industry technology roadmap, ESG", presentation dated November 14, 202499.3Â Â Â Â â€œEnd markets, wafer demand and lithography spending", presentation dated November 14, 202499.4Â Â Â Â â€œEUV products and business opportunity", presentation dated November 14, 202499.5Â Â Â Â â€œDUV products and business opportunity", presentation dated November 14, 202499.6Â Â Â Â â€œHolistic Lithography Solutions and business opportunity", presentation dated November 14, 202499.7Â Â Â Â â€œBusiness model and capital allocation strategy", presentation dated November 14, 202499.8Â Â Â Â â€œClosing remarks", presentation dated November 14, 2024SIGNATURESPursuant to the requirements of the Securities Exchange Act of 1934, the registrant has duly caused this report to be signed on its behalf by the undersigned, thereunto duly authorized.ASML HOLDING N.V. (Registrant)Date: November 18, 2024By:Â Â Â Â /s/ Christophe D. FouquetChristophe D. FouquetChief Executive Officer EX-99.1 2 exhibit991.htm EX-99.1 exhibit991 Confidential Skip Miller Opening remarks ASML Investor Day Veldhoven, The Netherlands November 14, 2024 Head of Investor Relations Small Talk 2024 Exhibit 99.1 Â Public Clear the isles, place bags under your seat Safety first Please locate your nearest emergency exit Page 2November 14, 2024 Â Public House rules November 14, 2024 Page 3 Please put your phone on silent or airplane mode Restroom locations In person and online Online audience can submit questions via the webcast player Presentations will be posted on our website shortly after the event Q&A Â Public Question & Answer session November 14, 2024 Page 4 Â Public Time Topic Presenter 12.00 â€“ 13.00 Registration & lunch 13.00 â€“ 13.05 Welcome & agenda Skip Miller 13.05 â€“ 13.50 Global market trends, Industry/Technology roadmaps and ESG Christophe Fouquet 13.50 â€“ 14.15 End markets, wafer demand and lithography spending Amit Harchandani 14.15 â€“ 14.40 EUV products and business opportunity Peter Vanoppen 14.40 â€“ 15.05 DUV products and business opportunity Herman Boom 15.05 â€“ 15.30 Break 15.30 â€“ 15.55 Holistic Lithography solutions and business opportunity Marco Pieters 15.55 â€“ 16.25 Business model and capital allocation strategy Roger Dassen 16.25 â€“ 16.35 Closing remarks Christophe Fouquet 16:35 â€“ 17:30 Q&A All presenters 17.30 End of formal program Agenda November 14, 2024 Page 5 Â Public Forward Looking Statements This document and related discussions contain statements that are forward-looking within the meaning of the U.S. Private Securities Litigation Reform Act of 1995, including statements with respect to our strategy, plans and expected trends, including trends in end markets and the technology industry and business environment trends, including the emergence of AI and its potential opportunities and expectations for the semiconductor industry, including computing power, advanced logic nodes and DRAM memory, statements with respect to Mooreâ€™s law and expected transistor growth and aspirations by 2030, global market trends and technology, product and customer roadmaps, long term outlook and expected lithography and semiconductor industry growth and trends and expected growth in semiconductor sales and semiconductor market opportunity through to 2030 and beyond, expected growth in wafer demand and capacity and additional wafer capacity requirements, expected investments by our customers, including investments in our technology and in wafer capacity, plans to increase capacity, expected growth in lithography spend, growth opportunities including opportunities for growth in service and upgrades and opportunities for growth in Installed Base Management sales, expected growth and gross margins in the holistic lithography business and expected addressable market for Applications products, expectations and benefits of a growing installed base, ASMLâ€™s and its supplierâ€™s capacity, expected production of systems, model scenarios and the updated model for 2030, including annual revenue and gross margin opportunity and development potential for 2030, outlook and expected, modelled or potential financial results, including revenue opportunity, gross margin, R&D costs, SG&A costs, capital expenditure, cash conversion cycle and annualized effective tax rate for 2030 and assumptions and drivers underlying such expected, modelled or potential amounts, and other assumptions underlying our business and financial models, expected trends, outlook and growth in semiconductor end markets and long term growth opportunities, demand and demand drivers, expected opportunities and growth drivers for and technological innovation of our products including DUV EUV, High NA, Hyper NA, Applications, and other products impacting productivity and costs, transistor dimensions, logic and DRAM shrink, foundry competition, statements with respect to dividends and share buybacks and our capital return policy, including expectation to return significant amounts of cash to shareholders through growing dividends and buybacks and statements with respect to energy generation and consumption trends and the drive toward energy efficiency, emissions reduction and greenhouse gas neutrality goals and target dates to achieve greenhouse gas neutrality, zero waste from operations and other ESG targets and ambitions and plans to maintain a leadership position in ESG, increasing technological sovereignty across the world and the expected impact on semiconductor sales, including specific goals of countries across the world, increasing competition in the foundry business, estimates for 2024 and other non-historical statements. You can generally identify these statements by the use of words like "may", "will", "could", "should", "project", "believe", "anticipate", "expect", "plan", "estimate", "forecast", "potential", â€œopportunityâ€, â€œscenarioâ€, â€œguidance,â€ "intend", "continue", "target", "future", "progress", "goal" and variations of these words or comparable words. These statements are not historical facts, but rather are based on current expectations, estimates, assumptions, models, opportunities and projections about our business and our future and potential financial results and readers should not place undue reliance on them. Forward- looking statements do not guarantee future performance and involve a number of substantial known and unknown risks and uncertainties. These risks and uncertainties include, without limitation, customer demand, semiconductor equipment industry capacity, worldwide demand for semiconductors and semiconductor manufacturing capacity, lithography tool utilization and semiconductor inventory levels, general trends and consumer confidence in the semiconductor industry and end markets, the impact of general economic conditions, including the impact of the current macroeconomic environment on the semiconductor industry, uncertainty around a market recovery including the timing thereof, the impact of inflation, interest rates, wars and geopolitical developments, the impact of pandemics, the performance of our systems, the success of technology advances and the pace of new product development and customer acceptance of and demand for new products, our production capacity and ability to adjust capacity to meet demand, supply chain capacity, timely availability of parts and components, raw materials, critical manufacturing equipment and qualified employees, our ability to produce systems to meet demand, the number and timing of systems ordered, shipped and recognized in revenue, risks relating to fluctuations in net bookings and our ability to convert bookings into sales, the risk of order cancellation or push outs and restrictions on shipments of ordered systems under export controls, risks relating to technology, product and customer roadmaps and Mooreâ€™s law, risks relating to the trade environment, import/export and national security regulations and orders and their impact on us, including the impact of changes in export regulations and the impact of such regulations on our ability to obtain necessary licenses and to sell our systems and provide services to certain customers, exchange rate fluctuations, changes in tax rates, available liquidity and free cash flow and liquidity requirements, our ability to refinance our indebtedness, available cash and distributable reserves for, and other factors impacting, dividend payments and share repurchases, the number of shares that we repurchase under our share repurchase programs, our ability to enforce patents and protect intellectual property rights and the outcome of intellectual property disputes and litigation, our ability to meet ESG goals and execute our ESG strategy, other factors that may impact ASMLâ€™s business or financial results including the risk that actual results may differ materially from the models, potential and opportunity we present for 2030 and other future periods, and other risks indicated in the risk factors included in ASMLâ€™s Annual Report on Form 20-F for the year ended December 31, 2023 and other filings with and submissions to the US Securities and Exchange Commission. These forward-looking statements are made only as of the date of this document. We undertake no obligation to update any forward-looking statements after the date of this report or to conform such statements to actual results or revised expectations, except as required by law. This document and related discussions contain statements relating to our approach to and interim progress on achieving certain energy efficiency and greenhouse gas emissions reduction targets, including our ambition to achieve greenhouse gas neutrality. References to â€œgreenhouse gas neutralâ€ means remaining emissions, after ASMLâ€™s efforts to reach its GHG emission reduction targets, compensated by the same amount of metric tons of carbon credits that are verified against recognised quality standards. Page 6November 14, 2024 Â Public Page 7November 14, 2024 Â Confidential THANK YOU Â EX-99.2 3 exhibit992.htm EX-99.2 exhibit992 Public Christophe Fouquet Global market trends Industry & ASML's technology roadmap ESG ASML Investor Day Veldhoven, The Netherlands November 14, 2024 President and Chief Executive Officer Small Talk 2024 Exhibit 99.2 Â Public â€¢ The Semiconductor Industry remains strong and Artificial Intelligence is expected to create further opportunity as major investments in supercomputing are happening and the entire industry is preparing to insert AI in all critical future applications â€¢ Our industry will require major innovations to address the anticipated cost and power consumption challenges of AI, and this will further boost the industry roadmap in a product mix shifting towards advanced logic and DRAM â€¢ Our customers remain at the core of our strategy, and we believe that lithography will remain at the heart of their innovation. We also anticipate that an increased number of critical lithography exposures for advanced logic and memory processes will continue to support our customers in addressing their challenges â€¢ We expect that our ability to 1- scale our EUV technology well into the next decade, 2- extend holistic lithography into supporting 3D front end integration and 3- improve the performance and cost effectiveness of our DUV products will continue to address all our customersâ€™ needs with a flexible and versatile portfolio â€¢ We will continue to leverage our large and growing systems installed base (DUV, EUV) to provide high value service and upgrades over a >20 years lifetime â€¢ ASML values the strong industry partnerships which are critical to our success and our collective commitment to a leadership position in ESG We expect that our ability to scale EUV technology into the next decade and extend our versatile holistic lithography portfolio could place ASML at the heart of the AI opportunity. This would continue to create significant growth in revenue and profitability in this decade. Page 2November 14, 2024 Â Public A Customer trust and partnership remains at the core of ASMLâ€™s strategy Seon-Yong Cha, SK Hynix CTO We expect that our ability to scale EUV technology into the next decade and extend our versatile holistic lithography portfolio could place ASML at the heart of the AI opportunity. This would continue to create significant growth in revenue and profitability in this decade. Page 3November 14, 2024 Â Public We see our society going from chips everywhere to AI chips everywhere Gen AI opens endless opportunities, expected to add 6-13T$ value to GDP by 2030 Connected world Climate change and resource scarcity Social and economic shifts Automation Healthcare, medical tech Technological sovereignty Working, learning remotely Cloud infrastructureHyperconnectivity Edge computing Energy transition Electrification, smart mobility Agricultural innovation Smarter use of limited resources Page 4*Source: McKinsey and Company, GenAI: The next S-curve for the semiconductor industry? | March 2024 Internet of Things November 14, 2024 Â Public Internet of Things Cloud infrastructure Edge computing Energy transition Automation Healthcare, medical tech Technological sovereignty Working, learning remotely Hyperconnectivity Electrification, smart mobility Agricultural innovation Smarter use of limited resources AI has strong potential to drive entire industry forward across many applications Mainstream markets grow in volume while high performance continues to follow Moore's law I-Line Advanced segments Mainstream segments Advanced segments Mainstream segments 300 mm 300 mm 300 mm 300 mm 300 mm 200 mm 300 mm 300 mm 200 mm 150 mm 300 mm ArFi KrF ArF DRAM NAND MPU ANALOG POWER OPTICAL SENSORS NON - OPTICAL SENSORS LOGIC Mainstream LOGICSPECIALTY MEMORY ADVANCED PACKAGING EUV US TW CN EU JP USKR IRL November 14, 2024 Page 5 Â Public Cloud infrastructure Edge computing Energy transition Automation Healthcare, medical tech Technological sovereignty Working, learning remotely Hyperconnectivity Electrification, smart mobility Agricultural innovation Smarter use of limited resources We reconfirm our view calling for global semi sales >$1T by 2030 Major investments are on-going in AI, the exact pace of its roll-out to consumer products is still unknown >1T$ 2030 Semi Sales 2015 100 200 300 400 500 600 700 800 900 1000 2016 2017 2018 2019 2020 2021 2022 2023 2024 Semi Sales [B $] 0 High performance compute 40% Other IoT Automotive Mobile Data AI power compute (+memory) Page 6 *Source: Kevin Zhang, TSMC, Semiconductor Industry: Present and Future, IEEE solid state Circuit Conference, Feb 2024 *Source: WSTS and Gartner Global data center and edge AI demands are expected to grow significantly year on year to represent >40% of semi sales demand in 2030 and generate some upside for our industry Connecting IoT Sensors Mainstream edge compute AI ? *Source: McKinsey and Company, GenAI: The next S-curve for the semiconductor industry? | March 2024November 14, 2024 Â Public Page 7 Semi Equipment Hardware ASML Peers Semi Non-Semi Loss in 2023 The semiconductor ecosystem has considerable means to drive innovation Despite a market downturn, the ecosystem generated over $865B EBIT in 2023 Logic IDM Foundry Wafers Distributor EDA Automotive PC Smartphone Contract Manufacturing Server Industrial Consumer Products Foundry Semi Peers Non-Semi Semi manufacturing Semi design Software and services Source: Corporate Marketing (CMKT) analysis; Company reports; Note: EBIT = Earnings before Interest & Taxes. Box size scales to EBITNovember 14, 2024 Â Public The semiconductor ecosystem has reinvested around half of its EBIT to drive long-term innovation and growth, and we expect this to continue Page 8 2015 2016 2017 EBIT [B $] 2018 437R & D [B $] 2019 2020 2021 2022 900 800 700 600 500 400 300 200 100 0 2023 449 540 616 564 616 883 817 865 197 220 252 289 318 348 404 468 504 Source: Corporate Marketing (CMKT) analysis; Company reports; Note: EBIT = Earnings before Interest & Taxes. 1046 2024e 541 1000 November 14, 2024 Â Public Mooreâ€™s law for computing power is alive and well Transistors per package continue to double every two years enabling one trillion by 2030 Source: nn Kelleher, ntel, â€œMooreâ€™s law â€“ now and in the futureâ€, ntel investor day Feb 17, 2022 Transistors Per Package (log) Aspiring to one trillion transistors by 2030 intel internal analysis of Intel products. Future projections based on products still in design. Future transistor counts are projections and are inherently uncertain. 2005 2010 2015 2020 2025 2030200019951990 Page 9 2x/2yrs November 14, 2024 Â Public High Performance Compute Demand Beyond Mooreâ€™s Law We expect that Generative AI will demand an acceleration of Mooreâ€™s law Energy use could set a ceiling on training capability moving forward if not addressed Page 10 Compute per package [FLOPs] 2x/2yrs Energy use per package [J] -0.6x/2yrs 2005 2010 2015 2020 2025 2030200019951990 Compute needs for AI Source: High Performance Computing: https://top500.org/lists/top500/ based on FP64 performance; Consumer GPU: nVidia & AMD data sheets based on FP32 performance Source: EPOCH , â€œ Notable modelsâ€ June 2024, updated Nov 2024 Energy Required for AI November 14, 2024 Â Public High Performance Compute Generative AI, high-performance computing power outpaces Mooreâ€™s law In 2030, >70% of data center demand could be driven by AI, representing >90% of Gen AI FLOPs Page 11 Compute per package [FLOPs] 2x/2yrs Energy use per package [J] -0.6x/2yrs 2005 2010 2015 2020 2025 2030200019951990 November 14, 2024 Source: High Performance Computing: https://top500.org/lists/top500/ based on FP64 performance; Consumer GPU: nVidia & AMD data sheets based on FP32 performance Source: EPOCH , â€œ Notable modelsâ€ June 2024, updated Nov 2024 Â Public Generative AI, high-performance computing power outpaces Mooreâ€™s law Supercomputer architecture has the potential to meet the needs of AI Page 12 High Performance Compute Compute [Flops] 2x/2yrs Mooreâ€™s law Energy use [J] (Energy per flop)-0.4x/2yrs Energy per flop + Compute Eff. -0.6x/2yrs 3x/2yrs Compute efficiency 2005 2010 2015 2020 2025 2030200019951990 Argonne Leadership Computing Facility: https://www.alcf.anl.gov/aurora High-performance computing Aurora supercomputer (HPC and AI applications) delivers 2,000,000,000,000,000,000 FLOPs November 14, 2024 Â Public Generative AI, high-performance computing power outpaces Mooreâ€™s law Architecture cost must be reduced to fully enable AI opportunity Aurora supercomputer (HPC and AI applications) delivers 2,000,000,000,000,000,000 FLOPs using ~85K CPUs/GPUS, >20PB memory for computing and >230PB memory for storage at ~500 M$ cost Cost: >500M$ Page 13Argonne Leadership Computing Facility: https://www.alcf.anl.gov/auroraNovember 14, 2024 Â Public Generative AI, high-performance computing power outpaces Mooreâ€™s law HPC rapidly growing energy consumption must be addressed to prevent a ceiling on training capability 1952 1960 1968 2008 2016 1023 1021 1019 1017 1015 1013 1011 109 107 105 103 101 Training compute (FLOPs) Deep learning era including feature extraction Large scale era combining complex datasets Argonne Leadership Computing Facility: https://www.alcf.anl.gov/aurora. | Source : Lisa Su, AMD, ITF May 21 2024 1025 2022 Generative AI Aurora supercomputer (HPC and AI applications) delivers 2,000,000,000,000,000,000 FLOPs using 60MW and 34,0 0 gallons of water per minute for cooling Energy consumption: >60MW Page 14November 14, 2024 Â Public Scalability of High-performance computing is endless.. â€¦ but new cost and energy challenges must be met to unleash AI opportunity AI computing architecture1 AI architecture cost2 The semiconductor industry needs to deliver the highest computing power / transistor density at the lowest cost, including the lowest possible CO2 emission Page 15 AI energy consumption3 Cost estimate: ~500M$2 exa FLOPS 60MW Source:Lisa Su, AMD, ITF May 21 2024 Argonne Leadership Computing Facility: https://www.alcf.anl.gov/aurora November 14, 2024 Â Public We expect AI applications to accelerate the need for advanced logic roadmap 2018 2020 2023 2025 2027 2029 2031 2033 2035 2037 2039 Future 2D and 3D innovations are paving the way for the next 15 years Page 16November 14, 2024 Â Public We expect AI applications to transform DRAM architecture and volume Future DRAM should integrate additional logic functionalities to improve performance & energy efficiency Page 17 â€œP M can improve performance and energy efficiency of memory-bound workloads by adding additional logic functionality to DR M memoryâ€ November 14, 2024 Â Public 10 100 1000 2015 2020 2025 2030 So, we continue to anticipate strong transistor growth for both logic and DRAM And we expect the semiconductor demand mix to shift towards advanced logic and DRAM Page 18 DRAM Gb produced [1018 / month] C GR â€™15-â€™23: 18% DRAM Source: Logic history: ASML end market model, DRAM history: WSTS, projections: ASML 10 100 1000 2015 2020 2025 2030 Transistors produced [1018 / month] C GR â€˜15-â€™23: 26% Logic November 14, 2024 Â Public Cost and energy reduction should be at the core of future process optimization 1. Increasing the number of good transistor processed at every step 2. Simplifying the overall process flow 3. Minimizing cost and emission of each processing step 40~80 cycles Page 19 Total cost and total emissions of wafer patterning must be reduced to support AI roadmap Total cost and emissions of wafer patterning can be reduced by: CO2 November 14, 2024 Â Public Page 201Source: ASML, excluding innovations in standard cell design Good printed transistor / â,¬ [a .u .] 1 ASML has delivered higher transistor density at lower cost for several decades We believe that EUV scalability & holistic lithography can extend our historical trend into the next decade (Critical layers) 2005 2010 2015 2020 2025 2030 2035 2040 Holistic lithography capability over time ArFi EUV 0.33 EUV 0.55 EUV 0.75 ArFi EUV 0.33 EUV 0.55 EUV 0.75 November 14, 2024 Â Public Page 211Source: ASML, excluding innovations in standard cell design Good printed transistor / â,¬ [a .u .] 1 ASML has delivered higher transistor density at lower cost for several decades We believe that EUV scalability & holistic lithography can extend our historical trend into the next decade (Critical layers) 2005 2010 2015 2020 2025 2030 2035 2040 Holistic lithography capability over time Overall November 14, 2024 Â Public 2024 2030 2024 2030 2024 2030 Good printed transistor CO2 Cost of Technology Environmental cost +150% /exposure - 30% /exposure - 50% /exposure EUV Extendibility ASMLâ€™s innovations can extend the benefits of EUV lithography More good transistors at lower cost and energy for customers, at increased profitability for ASML Page 22 = Good printed transistors Lithography Exposure cost CO2 Note: Cost / exposure reduction not taking into account possible inflation November 14, 2024 Â Public Page 23 = Good printed transistors Total lithography cost CO2 ASMLâ€™s innovations can extend the benefits of EUV lithography More good transistors at lower cost and energy for customers @ increased profitability for ASML November 14, 2024 Â Public Good printed transistors Resolution ProductivityAccuracyPatterning Yield Ã— Ã— Ã— Operational cost Environmental costSystem cost Lifetime/ + 1 Ton CO2 = 200 EUR + Total lithography cost ASML intends to innovate on all aspects to maximize its product portfolio value nnovation per product (EUV, DUVâ€¦) will target specific customer & market needs Page 24 = November 14, 2024 Â Public ACustomer trust and partnership remains at the core of ASMLâ€™s strategy Seon-Yong Cha, SK Hynix CTO We expect that our ability to scale EUV technology into the next decade and extend our versatile holistic lithography portfolio could place ASML at the heart of the AI opportunity. This would continue to create significant growth in revenue and profitability in this decade. Â Public We anticipate that semiconductor manufacturers will continue to drive shrink Reducing transistor dimensions likely remains the easiest way to drive density up at reduced cost Page 26 SP: Single Patterning, DP: Double Patterning, QP: Quadruple Patterning, EPE: Edge Placement Error Source: 1Luc van den Hove, IMEC , ITF May 21, 2024 0 5 10 15 30 20 25 21 18 16 14 28 5,2 4,3 3,5 3,5 Public data Customer projection 2020 2023 2025 2027 2029 2031 2033 2035 17 14 3,8 22 23 EPE [nm], Node , metal pitch , Linear scale Year of high-volume production 7 20392037 12 3 5 3 2 1.4 1.0 0.7 0.20.5 0.3 sub-0.2 Logic metal pitch [nm] Edge placement error

[nm] Uncertainty 5,5 4,5 5,8 Node name1 [nm] 40 Estimate November 14, 2024 Â Public Logic and DRAM are expected to drive further critical lithography exposures We expect EUV 0.33 NA layers to continue to increase node on node Page 27 2025 2029 - 2030 2025 2029 - 2030 high low high low low high NXE 0.33 NA low high # o f E U V 0 .3 3 N A E x p o s u re s # o f E U V 0 .3 3 N A E x p o s u re s 10-20% EUV spend CAGR 15-25% EUV spend CAGR DRAMLOGIC EUV lithography 0.33NA exposures (weighted average) EUV lithography 0.33NA exposures (weighted average) November 14, 2024 Â Public EUV 0.33 NA could enable further multi-patterning to single expose conversion Resulting in cost, yield and cycle time benefits for our customers Page 28 2022 2024 2026 2028 2030 2032 Single Expose (EUV 0.33 NA) A v e ra g e p a tt e rn in g c o s t p e r la y e r 2018 2020 LOGIC (LE-LE-LE â€“ layer) DRAM (SA-LE-LE - layer) LOGIC (LE-LE â€“ layer)2 1 3 Legend: LE = Litho-Etch | SA = Self aligned Cost of multi-patterning Cost of single expose November 14, 2024 Â Public EUV 0.33 NA could enable further multi-patterning to single expose conversion Resulting in higher number of EUV exposures for ASML between 2025 and 2030 Page 29 2022 2024 2026 2028 2030 2032 SE (EUV) A v e ra g e p a tt e rn in g c o s t p e r la y e r 64% 25% 17% 58% 33% 3% LE-LE-LE SE (EUV) LOGIC â€“ 5 layers 2 DRAM (DUV-EUV) 2025 2027 1 3x LE SE 2019 LOGIC (DUV-EUV) 2x LE SE 2028 LOGIC (DUV-EUV) 3 Litho CAPEX Litho OPEX Non Litho Ref. (SE DUV) SE DUV 4x SPACER 2x SPACER 2x LESE SE SE LOGIC (LE-LE-LE â€“ layer) DRAM (SA-LE-LE - layer) LOGIC (LE-LE â€“ layer) >4X >2X >1.5X>2X >1.5X increase in litho intensity % o f p a tt e rn in g c o s t Legend: LE = Litho-Etch | SA = Self aligned November 14, 2024 Â Public 0.55 NA EUV opportunity starts now as 0.33 NA EUV transitions to multi-patterning on <26nm pitch critical layers SP: Single Patterning, DP: Double Patterning, QP: Quadruple Patterning Source: 1Luc van den Hove, IMEC , ITF May 21, 2024 0 5 10 15 30 20 Single Expose 0.55 Double Expose 0.55 0.55 NA EUV ADOPTION OPPORTUNITYSingle Expose 0.33 Double Expose 0.3325 21 18 16 14 28 5,2 4,3 3,5 3,5 Public data Customer projection Estimate 2020 2023 2025 2027 2029 2031 2033 2035 17 14 3,8 22 23 E P E [n m], N o d e , m e ta l p it c h , L in e a r s c a le Year of high-volume production 7 20392037 12 3 5 3 2 1,4 1,0 0,7 0,20,5 0,3 sub-0.2 Logic metal pitch [nm] Edge placement error [nm] Uncertainty 5,5 4,5 5,8 Node name1 [nm] 40 Page 30November 14, 2024 Â Public LOGIC: High NA EUV enables more design freedom with 1.5D and 2D designs Single expose simplification reduces process steps, cycle time and improves yield Exposure NXE 1 Exposure NXE 2 Exposure NXE 3 P22 in horizontal direction combined with P28 in vertical direction. Page 31 This multi-exposure method is not performed in high-volume manufacturing due to its complexity. High NA Single Patterning Low NA Multi Patterning High NA Logic metal: ~35% cost benefit and process simplification Exposure High NA1 November 14, 2024 Â Public Logic and DRAM are expected to drive further critical lithography exposures Insertion of High NA in high volume manufacturing in 2026-27, adoption by end of the decade 2025 2029 - 2030 DRAMLOGIC 4-6 2-3 Expected average High NA Layers Page 32 2025 2029 - 2030 high low high low low high NXE 0.33 NA EXE 0.55 NA low high # o f E U V 0 .3 3 N A E x p o s u re s 4-9 EUV lithography 0.33NA Equivalent exposures (weighted average) >2030 # o f E U V 0 .3 3 N A E x p o s u re s >2030 >3 EUV lithography 0.33NA Equivalent exposures (weighted average) November 14, 2024 Â Public High NA EUVâ€™s latest optics innovation sets the base for our EUV roadmap Picometer stability (1/200 Si atom) achieved on asymmetric mirrors Page 33 NA >0.5 High NA Mirror Metrology at Zeiss Mask level Wafer level NA 0.33 Wafer level Mask level November 14, 2024 Â Public EUV source power continues to scale with opportunity to achieve >1000W 740W EUV power demonstrated EUV source power scaling 2010 2015 2020 2025 0 100 200 300 400 500 600 E U V s o u rc e p o w e r [W a tt s] Products 2030 700 800 900 1000 - measures identified to reach >1000W in the future 1 2 Research 1 EUV Plasma 1Î¼m Pre-Pulse 1Î¼m Rarefaction Pulse 10Î¼m Main Pulse 2 Plasma Process for 1 and 10 Âµm IR source Target Rarefied Target Tin Droplet 1Âµm architecture Droplet Repetition Rate Page 34November 14, 2024 Â Public High NA EUV optics support the vision of a higher productivity EUV platform EUV performance and productivity can be extended far into the next decade (>2030) 0.33 NA 0.55 NA 0.75 NA Today EXE platform NXE platform System commonality~50% ~95% Future: higher productivity platform Page 35November 14, 2024 Â Public 0.75 NA EUV opportunity is in the next decade when <16nm pitch will be needed Higher productivity platform can be designed to support future Hyper NA needs Page 36 SP: Single Patterning, DP: Double Patterning, QP: Quadruple Patterning Source: 1Luc van den Hove, IMEC , ITF May 21, 2024 Single Expose 0.75 0 5 10 15 30 20 25 21 18 16 14 28 5,2 4,3 3,5 3,5 Public data Customer projection Estimate 2020 2023 2025 2027 2029 2031 2033 2035 17 14 3,8 22 23 E P E [n m], N o d e , m e ta l p it c h , L in e a r s c a le Year of high-volume production 7 20392037 12 3 5 3 2 1,4 1,0 0,7 0,20,5 0,3 sub-0.2 Logic metal pitch [nm] Edge placement error [nm] Uncertainty 5,5 4,5 5,8 Node name1 [nm] 40 Multi Expose 0.75 0.75 NA EUV ADOPTION OPPORTUNITY Growing opportunity window for Logic beyond 2032 for replacing multi patterning 0.55 NA by 0.75 NA single patterning Double Expose 0.55 November 14, 2024 Â Public We expect front end 3D integration to complement 2D shrink in driving density Front end 3D integration challenges will trigger new litho opportunities for all semiconductor products Page 37 Stack LOGIC W-W hybrid W-W Fusion W-W | D-W Fusion Overlay 3D NAND BSPN CFET HVM 2026 >2032 Array CMOS Logic Bare-Si Logic Logic Bonding 5nm â†' 2nm50nm â†' 25nm 2.5nm â†' 1.6nm Litho KrF NXE/EXE NXE/EXE Array W-W / D-W hybrid Array CMOS 50nm â†' 25nm KrF NAND DRAM W-W hybrid W-W hybrid W-W / D-W hybrid 3D ARRAY4F2 2D ARRAY >2027 >2032 >2032 Array CMOS Array CMOS Array CMOS Array >4.5nm6nm â†' 3nm 6nm â†' 3nm ArFiArFi ArFi >2030 November 14, 2024 Â Public Holistic Lithography should support front end 3D integration Metrology and scanner control at pre and post bonding are critical process points needed for overlay Page 38 Pre-bonding CMOS Scanner correction and control ARRAY Scanner and offline metrology 2 1 Actuators Post-bondingBonding ARRAY CMOS Actuators large wafer deformation 3 Metrology Litho scanner Holistic lithography process control points Actuators 321 >5000 measurements/wafer 50 - 100nm overlay error >2000 measurements/wafer < 5 nm overlay error< 5 nm overlay error Holistic lithography to bring overlay error within spec massive metrology November 14, 2024 Â Public Lithography is a formidable tool to compensate process fingerprints Correction capability increased ~5 orders of magnitude, now @100 000 parameters per exposure Exposure stage 100% of wafers are measured 100% of wafers are processed field-by-field Metrology stage Even Fingers Odd Fingers Grey Filter X Y Z Optical Centerline Dose manipulator Flexible Illuminator Reticle stage 1975 1980 1985 1990 1995 2000 2005 2010 2015 2020 2025 1000 100 10 1 0.1 O v e rl a y [n m] 1,000 100 10 1 10,000 # u s e r s e le c ta b le l it h o c o rr e c ti o n s 100,000 Increasing correction capability per field, wafer, lot Scanner and Process Control Software November 14, 2024 Page 39 Â Public Wafer bonding can drive transistor density increase for DRAM memory 3 scenarios are currently in play for DRAM roadmap, all include bonding and require major innovations Page 40 2025 2026 2027 2028 2029 2030 2031 2032 2033 2034 2035 2036 D1c D1d D0a D0b D0c D0d D0e D0f 1) CBA: CMOS Bonded Array â€“ CMOS logic wafer bonded to the memory array 2) Stacking: Array bonding â€“ 2 or more memory array wafers bonded to each other. Wafer or die based 6F26F2 Source: Corporate Marketing (CMKT) analysis Â Public Wafer bonding can drive transistor density increase for DRAM memory 3 scenarios are currently in play for DRAM roadmap, all include bonding and require major innovations Page 41 2025 2026 2027 2028 2029 2030 2031 2033 2034 2035 2036 1c 1d 0a 0b 0c D0d D0e D0f 1) CBA: CMOS Bonded Array â€“ CMOS logic wafer bonded to the memory array 2) Stacking: Array bonding â€“ 2 or more memory array wafers bonded to each other. Wafer or die based 6F26F2 2032 6F2 + CBA 4F2 + CBA4F2 MEMORY CARRIER LOGIC Bonding MEMORY CARRIER LOGIC Bonding Source: Corporate Marketing (CMKT) analysisNovember 14, 2024 Â Public Wafer bonding can drive transistor density increase for DRAM memory 3 scenarios are currently in play for DRAM roadmap, all include bonding and require major innovations Page 42 2025 2026 2027 2028 2029 2030 2031 2033 2034 2035 2036 1c 1d 0a 0b 0c D0d D0e D0f 1) CBA: CMOS Bonded Array â€“ CMOS logic wafer bonded to the memory array 2) Stacking: Array bonding â€“ 2 or more memory array wafers bonded to each other. Wafer or die based 6F26F2 2032 6F2 + CBA 4F2 + CBA4F2 MEMORY CARRIER LOGIC Bonding MEMORY CARRIER LOGIC Bonding 3D Integration 0d 0e 0f Source: Corporate Marketing (CMKT) analysisNovember 14, 2024 Â Public Wafer bonding can drive transistor density increase for DRAM memory 3 scenarios are currently in play for DRAM roadmap, all include bonding and require major innovations Page 43 2025 2026 2027 2028 2029 2030 2031 2033 2034 2035 2036 1c 1d 0a 0b 0c 0d 0e 0f 1) CBA: CMOS Bonded Array â€“ CMOS logic wafer bonded to the memory array 2) Stacking: Array bonding â€“ 2 or more memory array wafers bonded to each other. Wafer or die based 6F26F2 4F2 + CBA4F2 2032 6F2 + CBA 3D Array ~>125 layers 2D Array 4F2 + CBA /Array 2D Array 6F2 + CBA /Array MEMORY CARRIER LOGIC MEMORY CARRIER LOGIC Bonding Bonding + Stacking Bonding Bonding + Stacking Bonding Source: Corporate Marketing (CMKT) analysisNovember 14, 2024 Â Public Bonding CBA Bonding Cost of technology remains a major criteria for our customersâ€™ roadmap choices EUV scalability and holistic lithography can support future front end 3D integration schemes Page 44 2023 2025 2027 2028 2030 2032 2034 2035 2037 2039 2041 B it c o s t s c a lin g ($ /G B) â€“ L o g s c a le 3D Array performance today; 5 layers 3D Array cost challenge performance of theoretical 125 layers if produced in HVM with todayâ€™s capability 6F2 / 4F2 6F2 3D Array insertion in 2032 requires 125 layers New DRAM factories New equipment 125 L New materials? 3D Array 2D Array Source: Corporate Marketing (CMKT) analysisNovember 14, 2024 Â Public Page 45 2023 2025 2027 2028 2030 2032 2034 2035 2037 2039 2041 3D Array performance today; 5 layers 3D Array cost challenge performance of theoretical 125 layers if produced in HVM with todayâ€™s capability 3D Array 6F2 / 4F2 6F2 3D Array insertion in 2032 requires 125 layers New DRAM factories New equipment 125 L CBA Bonding CBA Bonding + Stacking Bonding + Stacking Bonding Cost of technology remains a major criteria for our customersâ€™ roadmap choices EUV scalability and holistic lithography can support future front end 3D integration schemes 300 L New Materials? B it c o s t s c a lin g ($ /G B) â€“ L o g s c a le 2D Array Source: Corporate Marketing (CMKT) analysisNovember 14, 2024 Â Public ASML remains committed to its greenhouse gas neutrality ambitions Intensifying collaboration in the value chain aimed at accelerating climate action Page 46 Help society limit global temperature rise to 1.5Â°C Improvement lever 2025 2030 2040 2050 Paris Agreement Category Continue collaboration Collaborate to eliminate emissions from product use â–ª Improve energy efficiency of ASML products â–ª Support industry effort to improve access to affordable renewable energy, facilitating customers to source 100% renewable electricity by 2040 â–ª Collaborate as semiconductor industry to scale credible carbon removal options Collaborate to source GHG neutral products â–ª Set low-carbon design specifications â–ª Support transition to renewable energy â–ª Obtain commitment from suppliers to compensate any residual emissions from products to ASML as of 2030 G re e n h o u s e g a s n e u tra l G re e n h o u s e g a s n e u tra l Continue to drive energy efficiency & renewable energy â–ª Reduce energy use â–ª Use renewable energy â–ª Compensate any residual emissions as of 2025 â–ª Reduce energy use â–ª Use renewable energy â–ª Compensate any residual emissions as of 2025 G re e n h o u s e g a s n e u tra l G re e n h o u s e g a s n e u tra l S c o p e 1 & 2 S c o p e 3 Manufacturing & buildings Business travel & commuting Supply chain Product use Target Target Target This slide must be read in conjunction with, and is qualified by the disclosures set forth in, ASML's most recent Annual Report based on FRS and SMLâ€™s most recent nnual Report on Form 20-F filed with the U.S. Securities and Exchange Commission, including the Risk Factors in the Strategic Report with respect to dependencies upon emission reductions by third parties in our value chain and Appendix - Special note regarding emission targets Greenhouse gas neutral: Remaining emissions, after SMLâ€™s efforts to reach its GHG emission reduction targets, compensated by the same amount of metric tons of carbon credits that are verified against recognized quality standards Â Public 450 400 350 300 250 200 150 100 50 0 Our EUV innovations are also expected to drive EUV energy consumption down Within a 15 year period at customers, we anticipate 80% reduction of energy needed per wafer exposed 2018 2021 2023 2033 Improvement in energy per wafer Total power equivalent 100% Absolute Power Energy per Wafer 2025 2029 20312027 20% 100%

50% ATP throughput 30mJ [WPH] Wafers per hour Total power equivalent (kW) Total wafers per hour November 14, 2024 Page 47 Â Public Attractive & Inclusive communities STEM ESG innovation Employee giving Contribute to positive improvements and experiences in our communities Increase the talent pool that society needs to solve some of its key challenges Support innovative ideas to solve key ESG challenges Engage with and care for people in our communities ASML is increasing its engagement with communities SML and communities benefit from each otherâ€™s presence and support each otherâ€™s development November 14, 2024 Page 48 Â Public Forward Looking Statements This document and related discussions contain statements that are forward-looking within the meaning of the U.S. Private Securities Litigation Reform Act of 1995, including statements with respect to our strategy, plans and expected trends, including trends in end markets and the technology industry and business environment trends, including the emergence of AI and its potential opportunities and expectations for the semiconductor industry, including computing power, advanced logic nodes and DR M memory, statements with respect to Mooreâ€™s law and expected transistor growth and aspirations by 2030, global market trends and technology, product and customer roadmaps, long term outlook and expected lithography and semiconductor industry growth and trends and expected growth in semiconductor sales and semiconductor market opportunity through to 2030 and beyond, expected growth in wafer demand and capacity and additional wafer capacity requirements, expected investments by our customers, including investments in our technology and in wafer capacity, plans to increase capacity, expected growth in lithography spend, growth opportunities including opportunities for growth in service and upgrades and opportunities for growth in Installed Base Management sales, expected growth and gross margins in the holistic lithography business and expected addressable market for pplications products, expectations and benefits of a growing installed base, SMLâ€™s and its supplierâ€™s capacity, expected production of systems, model scenarios and the updated model for 2030, including annual revenue and gross margin opportunity and development potential for 2030, outlook and expected, modelled or potential financial results, including revenue opportunity, gross margin, R&D costs, SG&A costs, capital expenditure, cash conversion cycle and annualized effective tax rate for 2030 and assumptions and drivers underlying such expected, modelled or potential amounts, and other assumptions underlying our business and financial models, expected trends, outlook and growth in semiconductor end markets and long term growth opportunities, demand and demand drivers, expected opportunities and growth drivers for and technological innovation of our products including DUV EUV, High NA, Hyper NA, Applications, and other products impacting productivity and costs, transistor dimensions, logic and DRAM shrink, foundry competition, statements with respect to dividends and share buybacks and our capital return policy, including expectation to return significant amounts of cash to shareholders through growing dividends and buybacks and statements with respect to energy generation and consumption trends and the drive toward energy efficiency, emissions reduction and greenhouse gas neutrality goals and target dates to achieve greenhouse gas neutrality, zero waste from operations and other ESG targets and ambitions and plans to maintain a leadership position in ESG, increasing technological sovereignty across the world and the expected impact on semiconductor sales, including specific goals of countries across the world, increasing competition in the foundry business, estimates for 2024 and other non-historical statements. You can generally identify these statements by the use of words like "may", "will", "could", "should", "project", "believe", "anticipate", "expect", "plan", "estimate", "forecast", "potential", â€œopportunityâ€, â€œscenarioâ€, â€œguidance,â€ "intend", "continue", "target", "future", "progress", "goal" and variations of these words or comparable words. These statements are not historical facts, but rather are based on current expectations, estimates, assumptions, models, opportunities and projections about our business and our future and potential financial results and readers should not place undue reliance on them. Forward- looking statements do not guarantee future performance and involve a number of substantial known and unknown risks and uncertainties. These risks and uncertainties include, without limitation, customer demand, semiconductor equipment industry capacity, worldwide demand for semiconductors and semiconductor manufacturing capacity, lithography tool utilization and semiconductor inventory levels, general trends and consumer confidence in the semiconductor industry and end markets, the impact of general economic conditions, including the impact of the current macroeconomic environment on the semiconductor industry, uncertainty around a market recovery including the timing thereof, the impact of inflation, interest rates, wars and geopolitical developments, the impact of pandemics, the performance of our systems, the success of technology advances and the pace of new product development and customer acceptance of and demand for new products, our production capacity and ability to adjust capacity to meet demand, supply chain capacity, timely availability of parts and components, raw materials, critical manufacturing equipment and qualified employees, our ability to produce systems to meet demand, the number and timing of systems ordered, shipped and recognized in revenue, risks relating to fluctuations in net bookings and our ability to convert bookings into sales, the risk of order cancellation or push outs and restrictions on shipments of ordered systems under export controls, risks relating to technology, product and customer roadmaps and Mooreâ€™s law, risks relating to the trade environment, import/export and national security regulations and orders and their impact on us, including the impact of changes in export regulations and the impact of such regulations on our ability to obtain necessary licenses and to sell our systems and provide services to certain customers, exchange rate fluctuations, changes in tax rates, available liquidity and free cash flow and liquidity requirements, our ability to refinance our indebtedness, available cash and distributable reserves for, and other factors impacting, dividend payments and share repurchases, the number of shares that we repurchase under our share repurchase programs, our ability to enforce patents and protect intellectual property rights and the outcome of intellectual property disputes and litigation, our ability to meet ESG goals and execute our ESG strategy, other factors that may impact SMLâ€™s business or financial results including the risk that actual results may differ materially from the models, potential and opportunity we present for 2030 and other future periods, and other risks indicated in the risk factors included in SMLâ€™s nnual Report on Form 20-F for the year ended December 31, 2023 and other filings with and submissions to the US Securities and Exchange Commission. These forward-looking statements are made only as of the date of this document. We undertake no obligation to update any forward-looking statements after the date of this report or to conform such statements to actual results or revised expectations, except as required by law. This document and related discussions contain statements relating to our approach to and interim progress on achieving certain energy efficiency and greenhouse gas emissions reduction targets, including our ambition to achieve greenhouse gas neutrality. References to â€œgreenhouse gas neutralâ€ means remaining emissions, after SMLâ€™s efforts to reach its GHG emission reduction targets, compensated by the same amount of metric tons of carbon credits that are verified against recognised quality standards. Page 49November 14, 2024 Â Public THANK YOU Â EX-99.3 4 exhibit993.htm EX-99.3 exhibit993 Public Amit Harchandani ASML Investor Day Veldhoven, The Netherlands November 14, 2024 Senior Vice President & Head of Corporate Marketing Small Talk 2024 End Markets, Wafer Demand and Lithography Spending Exhibit 99.3 Â Public End Markets, Wafer Demand & Litho Spending The long-term outlook for the semiconductor industry remains promising, given the role of semis as mission-critical enablers of multiple megatrends. In particular, we believe that the emergence of AI creates a significant opportunity. As a result, we expect global semi sales to grow at 9% CAGR (2025-2030) & surpass $1tn by 2030. Key messages End Markets Wafer Demand Lithography Spending This end-market outlook translates into an overall wafer demand growth of 780K wafer starts per month per year (2025-2030). The rise of AI as a leading end driver also implies a positive mix-shift in the wafer demand profile from litho spending perspective. Lastly, we expect 5-8% extra overall wafer capacity by 2030 on top of demand-driven additions, owing to strategic considerations. We expect Advanced Logic & DRAM shrink to drive further EUV litho layers & spending. For Advanced Logic, we expect a gradual ramp of High NA (0.55NA) layers over 2025-2030, translating into an EUV litho spending CAGR of 10-20%. On the DRAM side, we expect an increase in both Low NA (0.33NA) and High NA (0.55NA) layers over 2025-2030, translating into an EUV litho spending CAGR of 15-25%. Â Public Estimate growth of our Installed Base business Installed Base Management Model assumptions Start with end markets Translate to worldwide litho spending, convert to ASML share Litho spend Convert to wafer demand: High â€“ Moderate â€“ Low scenarios Wafer demandEnd markets Scenarios â†' High â†' Moderate â†' Low 2030 Our model to determine the long-term opportunity for ASML This opportunity is driven by an interplay of market forces, tech choices & strategic considerations November 14, 2024 Page 3Source: ASML analysis Â Public Page 4 Our model to determine the long-term opportunity for ASML This opportunity is driven by an interplay of market forces, tech choices & strategic considerations November 14, 2024 Source: ASML analysis Â Public Page 5 MARKETS Our model to determine the long-term opportunity for ASML This opportunity is driven by an interplay of market forces, tech choices & strategic considerations November 14, 2024 Source: ASML analysis Â Public Page 6 MARKETS TECHNOLOGY Our model to determine the long-term opportunity for ASML This opportunity is driven by an interplay of market forces, tech choices & strategic considerations November 14, 2024 Source: ASML analysis Â Public Page 7 SCENARIOS PROBABILITY HIGHMODERATELOW Our model to determine the long-term opportunity for ASML This opportunity is driven by an interplay of market forces, tech choices & strategic considerations November 14, 2024 Source: ASML analysis Â Public Page 8 Scenarios â†' High â†' Moderate â†' Low 2030 Estimate growth of our Installed Base business Installed Base Management Model assumptions Start with end markets Translate to worldwide litho spending, convert to ASML share Litho spend Convert to wafer demand: High â€“ Moderate â€“ Low scenarios Wafer demandEnd markets Our model to determine the long-term opportunity for ASML This opportunity is driven by an interplay of market forces, tech choices & strategic considerations November 14, 2024 Source: ASML analysis Â Public Wafer Demand Lithography Spending End Markets Â Public The long-term outlook for the semiconductor industry remains promising Semiconductors serve as mission-critical enablers of multiple megatrends across society Page 10 Climate change and resource scarcity Social and economic shifts Automation Healthcare, medical tech Technological sovereignty Working, learning remotely Cloud infrastructure Hyperconnectivity Edge computing Energy transition Electrification, smart mobility Agricultural innovation Smarter use of limited resources Connected world November 14, 2024 Internet of Things Source: ASML analysis Â Public Page 11 We are particularly encouraged by the rapid progress in Artificial Intelligence We also see AI driving an increase in semiconductor sales as a % of global GDP, in the coming years Data AI power compute (+memory) Mainstream edge compute Sensors Connecting IoT AI Source: ASML analysis, International Monetary Fund (IMF), SEMINovember 14, 2024 PC Internet Smartphone AI 0.0% 0.2% 0.4% 0.6% 0.8% 1980 1990 2000 2010 2020 2030 Semiconductor sales as % of nominal GDP Semiconductor sales as % of global nominal GDP have steadily grown across the previous computing waves Â Public We see Servers, Datacenters & Storage as the key initial beneficiary of AI As a result, we now expect the semi sales associated with this end market crossing $350bn by 2030 AI Servers will account for a small share of overall units AI Servers will drive most of the growth & account for an increasing share of the semi sales, due to higher content Page 12 2025 2026 2027 2028 2029 2030 Server units (million) Standard Server AI Inference AI Training 2025 2026 2027 2028 2029 2030 Semiconductor sales ($bn) Standard Server AI Inference AI Training 4% 18% November 14, 2024 Source: ASML analysis Â Public Semi sales expected to grow at 9% CAGR (2025-2030) & surpass $1tn by 2030 Sharp increase in growth for Servers, Datacenters & Storage offsets most of moderation elsewhere Page 13 Smartphone ($bn) Wired & wireless Infrastructure ($bn) Automotive ($bn) Personal Computing ($bn) Servers, Datacenters & Storage ($bn) Industrial Electronics ($bn) Consumer Electronics ($bn) Total Semiconductor ($bn) 149 158 157 162 177 192 25 26 27 28 29 30 CMD 2022 CMD 2024 5% 92 100

100 101 106 112 25 26 27 28 29 30 4% 53 57 60 63 66 70 25 26 27 28 29 30 6% 70 72 74 78 80 83 25 26 27 28 29 30 3% 76 84 93 98 105 114 25 26 27 28 29 30 9% 84 91 98 100 110 120 25 26 27 28 29 30 7% 679 749 791 845 941 1051 25 26 27 28 29 30 9% 156 188 211 243 296 361 25 26 27 28 29 30 18% CMD 2022 CMD 2024 CMD 2022 CMD 2024 CMD 2022 CMD 2024 CMD 2022 CMD 2024 CMD 2022 CMD 2024 CMD 2022 CMD 2024 CMD 2022 CMD 2024 CMD 2022 CMD 2024 November 14, 2024 Source: ASML analysis Â Public End Markets Lithography Spending Wafer Demand Â Public Translating to expected growth of wafer demand in all segments Page 15Source: ASML analysisNovember 14, 2024 Â Public Translating to expected growth of wafer demand in all segments At CMD 2022, we saw a healthy overall wafer demand growth of ~760Kwspm/yr. (2025-2030) Page 16 CMD 2022 Million wafer starts/month (Mwspm) 6.7 8.6 2.1 3.21.9 2.2 2.1 2.6 2025 2030 Growth 2025-2030 (Kwspm/yr.) Mature Logic (>28nm) 380 Advanced Logic (<=28nm) 220 DRAM 60 NAND 100 Total wafer demand 760 12.8 16.6 November 14, 2024 Source: ASML analysis Â Public Translating to expected growth of wafer demand in all segments Off a lower 2025 level, we now expect overall wafer demand growth of ~780Kwspm/yr. (2025-2030) Page 17 CMD 2022 Million wafer starts/month (Mwspm) 6.7 8.6 2.1 3.21.9 2.2 2.1 2.6 2025 2030 Growth 2025-2030 (Kwspm/yr.) Mature Logic (>28nm) 380 Advanced Logic (<=28nm) 220 DRAM 60 NAND 100 Total wafer demand 760 CMD 2024 Million wafer starts/month (Mwspm) 5.8 7.5 2.0 3.21.7 2.5 1.7 1.9 2025 2030 Growth 2025-2030 (Kwspm/yr.) Mature Logic (>28nm) 340 Advanced Logic (<=28nm) 240 DRAM 160 NAND 40 Total wafer demand 780 12.8 16.6 11.2 15.1 November 14, 2024 Source: ASML analysis Â Public Translating to expected growth of wafer demand in all segments Going forward, we will classify Logic as Mainstream Logic (>7nm) and Advanced Logic (<=7nm) Page 18 CMD 2022 Million wafer starts/month (Mwspm) 6.7 8.6 2.1 3.21.9 2.2 2.1 2.6 2025 2030 Growth 2025-2030 (Kwspm/yr.) Mature Logic (>28nm) 380 Advanced Logic (<=28nm) 220 DRAM 60 NAND 100 Total wafer demand 760 CMD 2024 Million wafer starts/month (Mwspm) 5.8 7.5 2.0 3.21.7 2.5 1.7 1.9 2025 2030 Growth 2025-2030 (Kwspm/yr.) Mature Logic (>28nm) 340 Advanced Logic (<=28nm) 240 DRAM 160 NAND 40 Total wafer demand 780 CMD 2024 Million wafer starts/month (Mwspm) 7.1 9.0 0.7 1.7 1.7 2.5 1.7 1.9 2025 2030 Growth 2025-2030 (Kwspm/yr.) Mainstream Logic (>7nm) 380 Advanced Logic (<=7nm) 200 DRAM 160 NAND 40 Total wafer demand 780 (Old Logic classification) (New Logic classification) 12.8 16.6 11.2 15.1 11.2 15.1 November 14, 2024 Source: ASML analysis Â Public AI expected to drive stronger DRAM wafer demand growth towards 2030 We estimate that DRAM demand from AI Servers alone could reach ~1 million wspm by 2030 Page 19 Nvidia AI scaling roadmap: rapidly increasing HBM content AI-driven server DRAM wafer demand 2022 2023 2024 2025 2026 20272020 2021 Hopper Hopper 6S HBM3 94 GB 6S HBM3e 141 GB Blackwell 8S HBM3e 192 GB Blackwell Ultra 8S HBM3e 288 GB Ampere 5S HBM2e 80GB Rubin 8S HBM4 Rubin 12S HBM4 GB200 superchip Includes 2 Blackwell 2020 2022 2024 2026 2028 2030 W a fe r d e m a n d (M ill io n w a fe r s ta rt s p e r m o n th) DDR -Standard Server DDR-AI Server HBM - AI Server November 14, 2024 Source: Nvidia Investor presentation Oct 2024; ASML analysis Â Public Correlating wafer demand back to transistor & bit growth in the coming years We anticipate healthy growth rates over the period 2025-2030 for Advanced Logic & DRAM Page 20 Advanced Logic transistor growth 2025 2030 DRAM bit growth November 14, 2024 Source: ASML analysis 32% NAND bit growth 2025 2030 2025 2030 22% 26% Â Public Page 21 Wafer capacity will be driven by both wafer demand & strategic considerations November 14, 2024 Source: ASML analysis Â Public Wafer capacity will be driven by both wafer demand & strategic considerations Page 22 â€¢ $52bn investment â€¢ Tax credits US CHIPS and Science Act â€¢ $26bn investment â€¢ Tax credits JAPAN Strategy for Semiconductors â€¢ Government support via tax credits and loans SOUTH KOREA-Semiconductor Strategy â€¢ $48bn central government investment CHINA â€œBig Fundâ€ Phase 3 European Chips Act â€¢ $48bn investment â€¢ Tax credits â€¢ $9bn investment â€¢ Tax credits TAIWAN Chip-Based Industrial Innovation Program Firstly, technology sovereignty remains a tailwind with a broadening range of incentives November 14, 2024 INDIA Semiconductor Mission â€¢ $10bn government investment Source: Public announcements, FTI Consulting analysis and ASML analysis; Note: The overview is not exhaustive Â Public Secondly, the increased emphasis on supply security is evident from fabs coming online through 2027 Page 23 Europe / Middle EastAmericas Asia 1218 78 Coming fabs per region Wafer capacity will be driven by both wafer demand & strategic considerations November 14, 2024 Source: SEMI (November 2024), ASML analysis Â Public Lastly, at CMD 2022, we flagged foundry competition & talked about investments by our top-3 customers Page 24 U.S.A. U.S.A. U.S.A. Europe China Taiwan Korea Japan Wafer capacity will be driven by both wafer demand & strategic considerations November 14, 2024 Source: Public announcements, ASML analysis Â Public On balance, we still see competition as a tailwind today, as more customers announce their plans Page 25 U.S.A. U.S.A. U.S.A. U.S.A. U.S.A. Europe Europe China Taiwan Korea Korea Japan Japan Japan Wafer capacity will be driven by both wafer demand & strategic considerations November 14, 2024 Source: Public announcements, ASML analysis Â Public Wafer capacity will be driven by both wafer demand & strategic considerations As a result, we expect 5-8% extra overall capacity by 2030 on top of demand-driven additions Page 26 11.2 15.1 2025 2030 5-8% 5% â€¢ Tech sovereignty leading to less efficient use of the installed capacity as countries/regions aim to (re)gain fab footprint. â€¢ Increased emphasis on supply security resulting in geographically diversified ownership profile, in turn making load balancing more difficult. â€¢ Intensified competition could lead to a period with overcapacity as players try to capture market share. Strategic considerationsWafer capacity: Million wafer starts/month (Mwspm) Growth 2025-2030 (Kwspm/yr.) Total wafer demand 780 Strategic considerations 85 Total wafer capacity 865 November 14, 2024 Source: ASML analysis Â Public Wafer Demand End Markets Lithography Spending Â Public Advanced logic & DRAM shrink is expected to drive further layers & spending Increase in exposures, combined with wafer volume translates into double-digit EUV spending CAGRs Page 28 Advanced Logic: Average # of Total EUV Exposures* EUV litho spending CAGR (2025-2030): 10-20% November 14, 2024 Source: ASML analysis; Note: * EUV exposures are 0.33NA equivalents, which can also include 0.55NA exposures at a ratio of one 0.55NA exposure to two 0.33NA exposures 2025 2030 19-21 25-30 DRAM: Average # of Total EUV Exposures* EUV litho spending CAGR (2025-2030): 15-25% 2025 2030 5 7-10 4-6Expected average High NA (0.55NA) exposures 2-3Expected average High NA (0.55NA) exposures Â Public End Markets, Wafer Demand & Litho Spending The long-term outlook for the semiconductor industry remains promising, given the role of semis as mission-critical enablers of multiple megatrends. In particular, we believe that the emergence of AI creates a significant opportunity. As a result, we expect global semi sales to grow at 9% CAGR (2025-2030) & surpass $1tn by 2030. Key messages End Markets Wafer Demand Lithography Spending This end-market outlook translates into an overall wafer demand growth of 780K wafer starts per month per year (2025-2030). The rise of AI as a leading end driver also implies a positive mix-shift in the wafer demand profile from litho spending perspective. Lastly, we expect 5-8% extra overall wafer capacity by 2030 on top of demand-driven additions, owing to strategic considerations. We expect Advanced Logic & DRAM shrink to drive further EUV litho layers & spending. For Advanced Logic, we expect a gradual ramp of High NA (0.55NA) layers over 2025-2030, translating into an EUV litho spending CAGR of 10-20%. On the DRAM side, we expect an increase in both Low NA (0.33NA) and High NA (0.55NA) layers over 2025-2030, translating into an EUV litho spending CAGR of 15-25%. Â Public Forward Looking Statements This document and related discussions contain statements that are forward-looking within the meaning of the U.S. Private Securities Litigation Reform Act of 1995, including statements with respect to our strategy, plans and expected trends, including trends in end markets and the technology industry and business environment trends, including the emergence of AI and its potential opportunities and expectations for the semiconductor industry, including computing power, advanced logic nodes and DR M memory, statements with respect to Mooreâ€™s law and expected transistor growth and aspirations by 2030, global market trends and technology, product and customer roadmaps, long term outlook and expected lithography and semiconductor industry growth and trends and expected growth in semiconductor sales and semiconductor market opportunity through to 2030 and beyond, expected growth in wafer demand and capacity and additional wafer capacity requirements, expected investments by our customers, including investments in our technology and in wafer capacity, plans to increase capacity, expected growth in lithography spend, growth opportunities including opportunities for growth in service and upgrades and opportunities for growth in Installed Base Management sales, expected growth and gross margins in the holistic lithography business and expected addressable market for pplications products, expectations and benefits of a growing installed base, SMLâ€™s and its supplierâ€™s capacity, expected production of systems, model scenarios and the updated model for 2030, including annual revenue and gross margin opportunity and development potential for 2030, outlook and expected, modelled or potential financial results, including revenue opportunity, gross margin, R&D costs, SG&A costs, capital expenditure, cash conversion cycle and annualized effective tax rate for 2030 and assumptions and drivers underlying such expected, modelled or potential amounts, and other assumptions underlying our business and financial models, expected trends, outlook and growth in semiconductor end markets and long term growth opportunities, demand and demand drivers, expected opportunities and growth drivers for and technological innovation of our products including DUV EUV, High NA, Hyper NA, Applications, and other products impacting productivity and costs, transistor dimensions, logic and DRAM shrink, foundry competition, statements with respect to dividends and share buybacks and our capital return policy, including expectation to return significant amounts of cash to shareholders through growing dividends and buybacks and statements with respect to energy generation and consumption trends and the drive toward energy efficiency, emissions reduction and greenhouse gas neutrality goals and target dates to achieve greenhouse gas neutrality, zero waste from operations and other ESG targets and ambitions and plans to maintain a leadership position in ESG, increasing technological sovereignty across the world and the expected impact on semiconductor sales, including specific goals of countries across the world, increasing competition in the foundry business, estimates for 2024 and other non-historical statements. You can generally identify these statements by the use of words like "may", "will", "could", "should", "project", "believe", "anticipate", "expect", "plan", "estimate", "forecast", "potential", â€œopportunityâ€, â€œscenarioâ€, â€œguidance,â€ "intend", "continue", "target", "future", "progress", "goal" and variations of these words or comparable words. These statements are not historical facts, but rather are based on current expectations, estimates, assumptions, models, opportunities and projections about our business and our future and potential financial results and readers should not place undue reliance on them. Forward- looking statements do not guarantee future performance and involve a number of substantial known and unknown risks and uncertainties. These risks and uncertainties include, without limitation, customer demand, semiconductor equipment industry capacity, worldwide demand for semiconductors and semiconductor manufacturing capacity, lithography tool utilization and semiconductor inventory levels, general trends and consumer confidence in the semiconductor industry and end markets, the impact of general economic conditions, including the impact of the current macroeconomic environment on the semiconductor industry, uncertainty around a market recovery including the timing thereof, the impact of inflation, interest rates, wars and geopolitical developments, the impact of pandemics, the performance of our systems, the success of technology advances and the pace of new product development and customer acceptance of and demand for new products, our production capacity and ability to adjust capacity to meet demand, supply chain capacity, timely availability of parts and components, raw materials, critical manufacturing equipment and qualified employees, our ability to produce systems to meet demand, the number and timing of systems ordered, shipped and recognized in revenue, risks relating to fluctuations in net bookings and our ability to convert bookings into sales, the risk of order cancellation or push outs and restrictions on shipments of ordered systems under export controls, risks relating to technology, product and customer roadmaps and Mooreâ€™s law, risks relating to the trade

environment, import/export and national security regulations and orders and their impact on us, including the impact of changes in export regulations and the impact of such regulations on our ability to obtain necessary licenses and to sell our systems and provide services to certain customers, exchange rate fluctuations, changes in tax rates, available liquidity and free cash flow and liquidity requirements, our ability to refinance our indebtedness, available cash and distributable reserves for, and other factors impacting, dividend payments and share repurchases, the number of shares that we repurchase under our share repurchase programs, our ability to enforce patents and protect intellectual property rights and the outcome of intellectual property disputes and litigation, our ability to meet ESG goals and execute our ESG strategy, other factors that may impact SMLâ€™s business or financial results including the risk that actual results may differ materially from the models, potential and opportunity we present for 2030 and other future periods, and other risks indicated in the risk factors included in SMLâ€™s nnual Report on Form 20-F for the year ended December 31, 2023 and other filings with and submissions to the US Securities and Exchange Commission. These forward-looking statements are made only as of the date of this document. We undertake no obligation to update any forward-looking statements after the date of this report or to conform such statements to actual results or revised expectations, except as required by law. This document and related discussions contain statements relating to our approach to and interim progress on achieving certain energy efficiency and greenhouse gas emissions reduction targets, including our ambition to achieve greenhouse gas neutrality. References to â€œgreenhouse gas neutralâ€ means remaining emissions, after SMLâ€™s efforts to reach its GHG emission reduction targets, compensated by the same amount of metric tons of carbon credits that are verified against recognised quality standards. Page 30November 14, 2024 Â Public November 14, 2024 Page 31 THANK YOU Â EX-99.4 5 exhibit994.htm EX-99.4 exhibit994 Public Peter Vanoppen EUV Products and Business opportunity ASML Investor Day Veldhoven, The Netherlands November 14, 2024 Executive Vice President and Head of Business Line 0.55 NA EUV Small Talk 2024 Teun van Gogh Executive Vice President and Head of Business Line 0.33 NA EUV Exhibit 99.4 Â Public Key messages â€¢ EUV has reached high-volume manufacturing maturity providing a solid foundation for continued innovation. â€¢ The NXE:3800E offers a 38% improvement in productivity and 13% in overlay, with additional productivity and overlay improvements planned for the NXE:4000F and beyond. â€¢ The imec ASML High NA EUV lab opened in June, and all EUV customers have exposed critical layers. The data prove the capability of the system in lowering costs by 20-35% for critical layers compared to 0.33 NA, by dose reduction, enabling single exposure and 2D layout designs. â€¢ The first High NA EUV systems are operational at a customer, marking a key milestone in adoption of High NA EUV. â€¢ In the future both 0.33 NA and 0.55 NA EUV systems will be used for critical exposures. The EUV roadmap for the next decade includes the introduction of a high productivity platform and will enable affordable scaling for both 0.33 NA, 0.55 NA and potentially Hyper NA. â€¢ The growing installed base opportunity will be leveraged with a value- based service model in combination with productivity and performance upgrades. Â Public 13.5 EUV Wavelength [nm] 436 g-line 365 i-line 248 KrF 193 ArF and Immersion EUV lithography enabling a resolution improvement of 2 orders of magnitude to enable the most advanced chip manufacturing Page 3 R e s o lu ti o n [n m] 10 100 1000 1 1985 1990 1995 2000 2005 2010 2015 2020 2025 >2030 ArF (193nm) EUV 0.33 NA (13.5nm) EUV 0.55 NA (13.5nm) ArF Immersion (193nm) KrF (248nm) i-line (365nm) NA+67% NXT:1950i NXE:3400 EXE:5x00 XT:1400 NA+45% EUV 0.75 NA (13.5nm) NA+36% November 14, 2024 Â Public Page 4 20222018 24Q3: 93.5% 20202019 2021 Q1 Q2 Q3 Q4 Q1 Q2 Q3 Q4 Q1 Q2 Q3 Q4 Q1 Q2 Q3 Q4 2023 Q1 Q2 Q3 Q4 Q1Q4Q3 2024 Q2 W o rl d w id e A v a il a b il it y [%] 18Q4: 64% 19Q4: 82% 20Q4: 84% 21Q4: 87% 22Q4: 90% 23Q4: 93%Number of systems shipped (cumulative NXE:3400B/C, NXE:3600D, NXE:3800E) Availablity (total systems worldwide) Q3 Q4 N u m b e r o f s y s te m s s h ip p e d (c u m u la tiv e N X E :3 4 0 0 B /C , N X E :3 6 0 0 D & N X E :3 8 0 0 E)8545 53 55 62 76 923 8 11 5 12 7 0.33 NA EUV systems exceeding 93.5% worldwide average availability (Q3 2024) Moving towards 95% worldwide availability November 14, 2024 Â Public NXE productivity steadily increasing over the years NXE:3800E enabling the next big step in productivity for our customers Page 5 3500 3000 2500 2000 1500 1000 500 0 2018 20202019 2021 2022 2023 W a fe rs p e r d a y (W p D) 2024(Q3) 175 150 125 100 75 50 25 0 W a fe rs p e r h o u r (W p H) NXE:3400B NXE:3400C NXE:3600D 200 225 NXE:3800E 4000 4500 Max WpD for a single system - one day Max WpD for a single system - one week average 220 wph 160 wph 145* wph 137* wph * including Productivity Enhancement Package (PEP) November 14, 2024 Â Public NXE:3800E improves productivity from 160 to 220 WpH (+38%) and overlay by 13% to enable EUV on 2 nm node Page 6 Higher acceleration Reticle Stage Lower aberration Projection Optics optimized for stability at higher power 500W EUV Source operating at higher tin droplet frequency and with new tin management architecture Faster, double slotted load lock, Wafer Handler Higher acceleration Wafer Stages Reticle Clamp optimized for higher powers EXE / NXE common module NXE specific module * ASML acceptance test, overlay towards etched reference wafers, the NXE:3600D spec is 1.1nm Item NXE:3600D NXE:3800E Resolution 13 nm 13 nm Full wafer CDU â‰¤ 0.7 nm â‰¤ 0.7 nm Product Overlay â‰¤ 1.7 nm â‰¤ 1.5 nm Matched Overlay â‰¤ 1.1 nm â‰¤ 0.9 nm TpT at 30mJ/cm2 160 WpH 220 WpH Overlay Throughput November 14, 2024 Â Public30-Sep-2024 | 0.33 NA EUV systems for high volume manufacturing. 13215-2 | slide 7 Dedicated Chuck Overlay at 220 WpH NXE:3800E â€“ Dedicated chuck overlay 0.6 nm at 220 WpH, with spec at 0.8 nm Matched Machine Overlay shows expected performance improvement 1.6 1.4 1.2 1 0.8 0.6 0.4 0.2 0 Matched Machine Overlay population at 195 WpH: NXE:3400C, NXE:3600D, NXE:3800E NXE:3600D spec:1.1nm NXE:3400B/C spec:1.5nm N X E :3 8 0 0 E s p e c : 0 .9 n m [n m] Each bar represents a system qualification at ASML factory Overlay X: Overlay Y: 99.7% 0.5 nm 0.6 nm November 14, 2024 Page 7 Â Public EUV customers are installing NXE:3800E at their R&D and HVM sites from 2024 NXE:3800 installed at DRAM, LOGIC and Foundry customers Page 8 JP TW KR US November 14, 2024 Â Public Page 9 2023 2024 2025 2026 2027 2028 2029 2030 2031 2032 2033 Node (resolution) 0.7 nm2 nm 1.x nm 1 nm3 nm 0.5 nm 0.33NA 13 nm resolution NXE:3600D 1.1 nm | 160 WpH NXE:3800E MMO 0.9 nm | 220 WpH NXE:4000F MMO <0.8 nm | â‰¥ 250 WpH NXE:4200G â‰¥ 280 WpH MMO = Matched-Machine Overlay (0.33NA throughput at 30 mJ/cm2 dose) Reticle Stage With 25% increase in acceleration 1Âµm PP / RP* 600W source supporting increased productivity Wafer Stage Reduced wafer exchange overhead NXE:3800E NXE:4000F Power 500W 600W Throughput 220 WpH 250 WpH Product Overlay â‰¤ 1.5 nm â‰¤ 1.3 nm Matched Overlay â‰¤ 0.9 nm â‰¤ 0. 8 nm NXE:4000F productivity increase with common source, EXE wafer stage technology and evolutionary reticle stage acceleration increase. Common technology with NXE NXE:next NXE:4000F specified at â‰¥250 WpH and 0.8 nm Matched Machine Overlay Enables improvements in both productivity (14%) and overlay to enable 0.33 NA EUV on the 1.4 nm node *PP pre-pulse / RP rarefaction pulse November 14, 2024 Â Public Good printed transistors Resolution ProductivityAccuracyPatterning Yield Ã— Ã— Ã— Operational cost Environmental costSystem cost Lifetime/ + 1 Ton CO2 = 200 EUR + Total lithography cost ASML will innovate in EUV to lower the cost of good printed transistors Our portfolio with 0.33 NA, 0.55 NA and potentially Hyper NA will provide full flexibility to our customers Page 10 = November 14, 2024 Â Public High NA EUV opportunity starts now as 0.33 NA EUV transitions to multi-patterning on <26nm pitch critical layers SP: Single Patterning, DP: Double Patterning, QP: Quadruple Patterning Source: 1Luc van den Hove, IMEC , ITF May 21, 2024 0 5 10 15 30 20 Single Expose 0.55 Double Expose 0.55 0.55 NA EUV ADOPTION OPPORTUNITYSingle Expose 0.33 Double Expose 0.3325 21 18 16 14 28 5,2 4,3 3,5 3,5 Public data Customer projection Estimate 2020 2023 2025 2027 2029 2031 2033 2035 17 14 3,8 22 23 E P E [n m], N o d e , m e t a l p it c h , L in e a r s c a le Year of high-volume production 7 20392037 12 3 5 3 2 1,4 1,0 0,7 0,20,5 0,3 sub-0.2 Logic metal pitch [nm] Edge placement error [nm] Uncertainty 5,5 4,5 5,8 Node name1 [nm] 40 Page 11November 14, 2024 Â Public High NA EUV â€“ Introducing high-resolution, high-contrast imaging technology The latest addition to SMLâ€™s holistic lithography roadmap High NA EUV Lithography â€¢ Best-in-class overlay performance â€¢ High-contrast imaging for LCDU gain â€¢ Single expose vs. multi- patterning â€¢ High contrast imaging for lower dose â€¢ High contrast â€¢ 2.8x improvements in density â€¢ Process simplification â€¢ Increased design flexibility, 2D patterns Resolution ProductivityAccuracyPatterning Yield = Single expose EXE LE â€“ LE NXE Non-litho Litho opex Litho capex Legend: LE = Litho-Etch 1.2X Page 12November 14, 2024 Â Public High NA EUV technical values and customer benefits Page 13 Customer benefitsHigh NA technical values Less mask = less patterning process defects Process simplification, improved edge placement error Reduced defect density by Patterning cost reduction by Enabling single patterning (from multi patterning) Dose reduction with higher contrast (productivity) Enabling 2D designs (device cell shrink) 1) 2) 3) 1-2 days saved per mask reduction Shorter cycle time Less patterning fab space 0.55 NA higher resolution enables 1.7x smaller features and 2.8x increased density Higher imaging contrast enables 40% improvement in Local CDU 1.4x reduced pattern variability at 1.4x lower dose 0 55 November 14, 2024 Â Public A decade of development leading to the opening of the joint imec ASML Lab in June 2024 France: milling body US: short stroke reticle stage Netherlands: 700m2 High-NA assembly building openedFrance: New facilities for large frame welding Germany: New facilities for optic metrology Module integration 2020-2022 Module qualification 2022-2023 2023-2024 System qualification 2024 > Wafer exposures 2018-2021 Module Manufacturing Design system 2014-2018 Anamorphic design San Diego: Source qualification Germany Illuminator integration Veldhoven: qualification waferstage Wilton: qualification reticlestage Veldhoven System integration Joint Lab Page 14November 14, 2024 Â Public Litho Cluster: system install ongoing and track qualified High NA scanner Metrology Room Track IMEC / ASML High NA Lab supporting future insertion High NA lab provides early access to all EUV customers Page 15 Public Â Public Customers have exposed critical layers in High NA EUV lab & verified the benefits Progress on High NA recognized and its importance in enabling cost effective scaling acknowledged Page 16 Mark Philips (Intel) reports on High NA at SPIE photomask technology, September 2024 In total >10,000 wafers exposed on the high NA systems including >1300 DRAM and Foundry customer wafers in the lab, expecting to reach ~2000 wafers by the end of the year 2000 1750 1500 1250 1000 750 500 500 250 0 Q2 Q3 Q4 Today # la b w a fe rs e x p o s e d 2024 DRAM FOUNDRY November 14, 2024 Â Public In total >10,000 wafers exposed on the high NA systems including >1300 DRAM and Foundry customer wafers in the lab, expecting to reach ~2000 wafers by the end of the year 2000 1750 1500 1250 1000 750 500 500 250 0 Q2 Q3 Q4 Today # la b w a fe rs e x p o s e d 2024 DRAM FOUNDRY Customers have exposed critical layers in High NA EUV lab & verified the benefits Progress on High NA recognized and its importance in enabling cost effective scaling acknowledged Page 17 Mark Philips (Intel) reports on High NA at SPIE photomask technology, September 2024 â€¢ High NA EUV is here: healthy tools, available in the field, with a full suite of holistic applications â€¢ The ecosystem is ready to support process development: reticles, resists, underlayers, etches, OPC and metrology â€¢ The expected benefits of higher NA are evident in resist images â€¢ The timing is right to avoid the cost and complexity of excessive mask splits with 0.33 NA EUV Mark Philips November 14, 2024 Â Public High NA EUV high-contrast imaging increases process window while reducing dose requirements and patterning defects resulting in higher productivity and better yield x-position [nm] threshold NA=0.55 x-position [nm] A e ri a l im a g e i n te n s it y [a u] NA=0.33 threshold 0.33 0.55 Page 18 NA 0.55 NA 0.33 A e ri a l im a g e i n te n s it y [a u] November 14, 2024 Â Public High NA EUV offers a new design opportunity going for 2D design layouts This enables higher logic cell density (hence scaling) and optimized routing of interconnect layers reducing the total number of metal layers Page 19 0.33 NA 0.55 NA 0.55 NA resolution and contrast enables single expose of 2D metal, replacing two metal and one via layers Two metal layers (1D) and additional Via layer required to connect 3 transistors P22 in horizontal direction combined with P28 in vertical direction 0.55 NA single expose image Metal 1 Vertical Metal 2 horizontal Via 1 3 2 1 2D Metal Contact to transistor 1 3 2 Contact to transistor1 November 14, 2024 Â Public High NA EUV exposures on contact hole patterns (DRAM layer) through pitch show higher contrast, resulting in improved LCDU and reduced dose Page 20 P40 P36 P34 P32 P30 0.33 NA 0.55 NA LCDU Dose LCDU Dose 2.4 nm 2.6 nm 2.7 nm 3.0 nm 3.6 nm 63 mJ/cmÂ² 66 mJ/cmÂ² 66 mJ/cmÂ² 72* mJ/cmÂ² 73* mJ/cmÂ² Based on 40nm CAR P28 1.4 nm 1.5 nm 1.6 nm 1.7 nm 2.0 nm 48 mJ/cmÂ² 53 mJ/cmÂ² 47 mJ/cmÂ² 51 mJ/cmÂ² 45 mJ/cmÂ² 2.3 nm 45 mJ/cmÂ² *23% illuminator efficiency November 14, 2024 Â Public High NA EUV exposures on contact hole patterns (DRAM layer) through pitch show higher contrast, resulting in improved LCDU and reduced dose Page 21 P40 P36 P34 P32 P30 0.33 NA 0.55 NA LCDU Dose LCDU 2.4 nm 2.6 nm 2.7 nm 3.0 nm 3.6 nm Based on 40nm CAR P28 1.4 nm 1.5 nm 1.6 nm 1.7 nm 2.0 nm 48 mJ/cmÂ² 53 mJ/cmÂ² 47 mJ/cmÂ² 51 mJ/cmÂ² 45 mJ/cmÂ² 2.3 nm 45 mJ/cmÂ² Dose at same LCDU as 0.55 NA 191 mJ/cmÂ² 209 mJ/cmÂ² 193 mJ/cmÂ² 220* mJ/cmÂ² 238* mJ/cmÂ² *23% illuminator efficiency November 14, 2024 Â Public High NA EUV exposures on contact hole patterns (DRAM layer) through pitch show higher contrast, resulting in improved LCDU and reduced dose Page 22 P40 P36 P34 P32 P30 0.33 NA 0.55 NA LCDU Dose LCDU 2.4 nm 2.6 nm 2.7 nm 3.0 nm 3.6 nm Based on 40nm CAR P28 1.4 nm 1.5 nm 1.6 nm 1.7 nm 2.0 nm 48 mJ/cmÂ² 53 mJ/cmÂ² 47 mJ/cmÂ² 51 mJ/cmÂ² 45 mJ/cmÂ² 2.3 nm 45 mJ/cmÂ² Dose at same LCDU as 0.55 NA The cost benefit of high NA is 50% compared to a low NA exposure at the same LCDU Cost benefit 49% 50% 50% N.A. N.A. 191 mJ/cmÂ² 209 mJ/cmÂ² 193 mJ/cmÂ² 220* mJ/cmÂ² 238* mJ/cmÂ² *23% illuminator efficiency November 14, 2024 Â Public LOGIC [P19]: High NA EUV single exposure will enable ~35% cost benefit and significant process simplification compared to multi patterning 0.33 NA EUV Page 23 Exposure 0.55 NA Litho etch 0.33 NA Multi Patterning 0.55 NA Single Patterning Exposure 0.33 NA 1 Exposure 0.33 NA 2 Exposure 0.33 NA 3 Litho etch Litho etch Cut T2T ~15 nm | After etchP19 1 Cost benefit is calculated based on throughput and estimated non-litho cost. November 14, 2024 Â Public LOGIC [P30]: ~20% cost benefit and process simplification moving from double exposure 0.33 NA EUV to single exposure High NA EUV Page 24 Center to center 30 nm Random Via 0.33 NA Multi Patterning 0.55 NA Single Patterning Exposure 0.55 NA 1 High NA single exposure image Exposure 0.33 NA 1 Exposure 0.33 NA 2 Cost benefit is calculated based on throughput and estimated non-litho cost. November 14, 2024 Â Public LOGIC [P36]: Higher contrast enables lower exposure dose at better imaging quality resulting in higher productivity and lower cost Page 25 Single exposure comparison (Logic Via layer, 18 nm holes, pitch 36 nm) 0.33 NA CD uniformity (LCDU) NXE EXE Deformed Contact Holes Defect free Contact Holes 0.55 NA Dose 250 mJ/cm2 52 wafers/hour pupil pupil Dose 77 mJ/cm2 136 wafers/hour November 14, 2024 Â Public DRAM 15nm contact holes: High NA enables high productivity single exposure Moving from triple exposure (2x 0.33NA EUV +1x DUV) to single exposure 0.55 NA EUV Page 26 CD SEM picture: 15 nm contact holes (after development) 0.33 NA + DUV Multi Patterning 0.55 NA Single Patterning Exposure 0.33 NA 1 Exposure 0.33 NA 2 Exposure DUV 3 Exposure 0.55 NA 1 Litho etch 0.55 NA single exposure image Cost benefit is calculated based on throughput and estimated non-litho cost. | *depending on CD SEM settings and post processing Litho etch Litho etch Trim Main etch High NA DRAM Capacitor: ~30% cost benefit and process simplification November 14, 2024 Â Public DRAM 15 nm contact holes: Higher contrast of High NA enables lower exposure dose at better imaging quality, resulting in higher productivity and lower cost Page 27 Single exposure comparison (DRAM capacitor layer, 15 nm holes) 0.33 NA CD uniformity (LCDU) NXE EXE Pupil for 0.33NA exposure enables only 23% of light to be used, reducing productivity Deformed Contact Holes Defect free Contact Holes 0.55 NA Pupil for 0.55NA exposure enables the full 100% of light to be used, maintaining full productivity Dose 148 mJ/cm2 22 wafers/hour Dose 44 mJ/cm2 155 wafers/hour November 14, 2024 Â Public High NA half field exposure requires stitching for large die Engineering solutions available to enable at resolution stitching Page 28 14nm lines (28nm pitch) 12nm lines (24nm pitch) Initial EXE exposures show the feasibility of stitching A and B field together 0.33NA Full Field 0.55NA Half Field Field with multiple small die Mask A Mask B Field with single large die Twice the number of fields exposed using the same mask; no stitching needed Image is split between two masks; stitching of the pattern may be needed Mask A Mask A B A November 14, 2024 Â Public EUV product roadmap enabling affordable scaling Towards high productivity platform for 0.33NA EUV, 0.55NA EUV and potentially hyper NA in the next decade Page 29 2023 2024 2025 2026 2027 2028 2029 2030 2031 2032 2033 Node (resolution) 0.7 nm2 nm 1.x nm 1 nm3 nm 0.5 nm 0.55 NA 8 nm resolution EXE:5200B MMO <0.8 nm | 175 WpH EXE:5000 1.1 nm | 110 WpH EXE 5200C MMO <0.8 nm | â‰¥ 185 WpH EXE:5400D â‰¥ 95 WpH EXE High Productivity NEXT NXE High Productivity NEXT Hyper NA opportunity High Productivity common platform 30%Cost per exposure MMO = Matched-Machine Overlay 0.33NA throughput at 30 mJ/cm2 dose 0.55NA throughput at 50 mJ/cm2 dose 0.33NA 13 nm resolution NXE:3600D 1.1 nm | 160 WpH NXE:3800E MMO 0.9 nm | 220 WpH NXE:4000F MMO <0.8 nm | â‰¥ 250 WpH NXE:4200G â‰¥ 280 WpH NXE:next EXE:next OEE (overall equipment efficiency) and productivity Continued improvement November 14, 2024 Â Public High productivity common platform is enabled by going to one modular frame architecture Modular Machine Support Frame allows for product mix flexibility in fabs â€¢ Common Source â€¢ Common interfaces/modules â€¢ Common High Transmission High Flexible Illuminator â€¢ Shared innovations in stage accelerations to enable high productivity Low NA (0.33) Common modules Product Specific modules Low NA Frame adaptors High NA (0.55) Flexible pedestal position High NA Hyper NA (0.75) Î” Tracing Hyper NA Î” Object Image shift change Page 30November 14, 2024 Â Public EUV source power continues to scale with opportunity to achieve >1000W 740W EUV power demonstrated - measures identified to reach >1000W in the future EUV source power scaling 2010 2015 2020 2025 0 100 200 300 400 500 600 EUV-source power [Watts] Products 2030 700 800 900 1000 1 2 Research 1 EUV Plasma 1Î¼m Pre-Pulse 1Î¼m Rarefaction Pulse 10Î¼m Main Pulse 2 Plasma Process for 1 and 10 Âµm IR source Target Rarefied Target Tin Droplet 1Âµm architecture Droplet Repetition Rate Page 31November 14, 2024 Â Public High transmission optics for 0.33 NA and 0.55 NA enable a significant step in productivity High transmission optics are enabled on the high productivity common platform Page 32 0.55 NA Flexible illuminator: â–ª Enable ~1.4x increase in transmission â–ª Productivity scaling of productivity towards 300 WpH â–ª Enable improved contrast and extension of resolution limits â–ª Enable common vertical source angle High Transmission POB on 0.33NA Flexible illuminator on 0.55NA 0.33 NA high transmission POB: â–ª Enable >2x increase in transmission â–ª Enable scaling of productivity >450 WpH â–ª Enable common vertical source angle November 14, 2024 Â Public Innovation in optics, source and stages enables scaling of EUV productivity Single patterning 0.55 NA EUV will outperform double patterning 0.33 NA EUV in productivity Page 33Graph shows product name / throughput in WpH 500 550 450 400 350 300 250 Throughput [WpH] 200 150 100 50 0 2015-2020 2020-2025 2030-20352025-2030 NXE:3400B NXE:3400C NXE:3600D NXE:3800E NXE:4000F NXE:4200G 0.33 NA single expose (30 mJ/cm2) 0.33 NA: High Productivity Platform Estimate 0.33 NA double expose (30 mJ/cm2) 0.55 NA single expose (50 mJ/cm2) 0.55 NA: High Productivity Platform EXE:5000 EXE:5200B EXE:5400D EXE:5200C 0.33 NA: High Productivity Platform Estimate Estimate November 14, 2024 Â Public EUV Installed Base will further grow in coming years, >20 years lifetime anticipated ASML supports customers to optimize output of their 0.33 NA EUV & 0.55 NA EUV installed base over lifetime Page 34 Availability (Service) Life cycle extension (Service) Upgrades Cost per Exposure (Service) Increase fleet availability Reduce machine long downs Performance extension Increase system capability Cost roadmap over lifetime Standardize service actions over NXE and EXE Upgrade machines to extend lifetime Relative sales over the scanner lifetime 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 0% 50% 100% 150% 200% 250% Years Upgrades and service System sales 300% Over 20 years, service & upgrades expected to add significant value for customers and ASML November 14, 2024 Â Public Key messages â€¢ EUV has reached high-volume manufacturing maturity providing a solid foundation for continued innovation. â€¢ The NXE:3800E offers a 38% improvement in productivity and 13% in overlay, with additional productivity and overlay improvements planned for the NXE:4000F and beyond. â€¢ The imec ASML High NA EUV lab opened in June, and all EUV customers have exposed critical layers. The data prove the capability of the system in lowering costs by 20-35% for critical layers compared to 0.33 NA, by dose reduction, enabling single exposure and 2D layout designs. â€¢ The first High NA EUV systems are operational at a customer, marking a key milestone in adoption of High NA EUV. â€¢ In the future both 0.33 NA and 0.55 NA EUV systems will be used for critical exposures. The EUV roadmap for the next decade includes the introduction of a high productivity platform and will enable affordable scaling for both 0.33 NA, 0.55 NA and potentially Hyper NA. â€¢ The growing installed base opportunity will be leveraged with a value- based service model in combination with productivity and performance upgrades. Â Public Forward Looking Statements This document and related discussions contain statements that are forward-looking within the meaning of the U.S. Private Securities Litigation Reform Act of 1995, including statements with respect to our strategy, plans and expected trends, including trends in end markets and the technology industry and business environment trends, including the emergence of AI and its potential opportunities and expectations for the semiconductor industry, including computing power, advanced logic nodes and R M memory, statements with respect to Mooreâ€™s law and expected transistor growth and aspirations by 2030, global market trends and technology, product and customer roadmaps, long term outlook and expected lithography and semiconductor industry growth and trends and expected growth in semiconductor sales and semiconductor market opportunity through to 2030 and beyond, expected growth in wafer demand and capacity and additional wafer capacity requirements, expected investments by our customers, including investments in our technology and in wafer capacity, plans to increase capacity, expected growth in lithography spend, growth opportunities including opportunities for growth in service and upgrades and opportunities for growth in Installed Base Management sales, expected growth and gross margins in the holistic lithography business and expected addressable mar et for pplications products, expectations and benefits of a growing installed base, SMLâ€™s and its supplierâ€™s capacity, expected production of systems, model scenarios and the updated model for 2030, including annual revenue and gross margin opportunity and development potential for 2030, outlook and expected, modelled or potential financial results, including revenue opportunity, gross margin, R&D costs, SG&A costs, capital expenditure, cash conversion cycle and annualized effective tax rate for 2030 and assumptions and drivers underlying such expected, modelled or potential amounts, and other assumptions underlying our business and financial models, expected trends, outlook and growth in semiconductor end markets and long term growth opportunities, demand and demand drivers, expected opportunities and growth drivers for and technological innovation of our products including DUV EUV, High NA, Hyper NA, Applications, and other products impacting productivity and costs, transistor dimensions, logic and DRAM shrink, foundry competition, statements with respect to dividends and share buybacks and our capital return policy, including expectation to return significant amounts of cash to shareholders through growing dividends and buybacks and statements with respect to energy generation and consumption trends and the drive toward energy efficiency, emissions reduction and greenhouse gas neutrality goals and target dates to achieve greenhouse gas neutrality, zero waste from operations and other ESG targets and ambitions and plans to maintain a leadership position in ESG, increasing technological sovereignty across the world and the expected impact on semiconductor sales, including specific goals of countries across the world, increasing competition in the foundry business, estimates for 2024 and other non-historical statements. You can generally identify these statements by the use of words like "may", "will", "could", "should", "project", "believe", "anticipate", "expect", "plan", "estimate", "forecast", "potential", â€œopportunityâ€, â€œscenarioâ€, â€œguidance,â€ "intend", "continue", "target", "future", "progress", "goal" and variations of these words or comparable words. These statements are not historical facts, but rather are based on current expectations, estimates, assumptions, models, opportunities and projections about our business and our future and potential financial results and readers should not place undue reliance on them. Forward- looking statements do not guarantee future performance and involve a number of substantial known and unknown risks and uncertainties. These risks and uncertainties include, without limitation, customer demand, semiconductor equipment industry capacity, worldwide demand for semiconductors and semiconductor manufacturing capacity, lithography tool utilization and semiconductor inventory levels, general trends and consumer confidence in the semiconductor industry and end markets, the impact of general economic conditions, including the impact of the current macroeconomic environment on the semiconductor industry, uncertainty around a market recovery including the timing thereof, the impact of inflation, interest rates, wars and geopolitical developments, the impact of pandemics, the performance of our systems, the success of technology advances and the pace of new product development and customer acceptance of and demand for new products, our production capacity and ability to adjust capacity to meet demand, supply chain capacity, timely availability of parts and components, raw materials, critical manufacturing equipment and qualified employees, our ability to produce systems to meet demand, the number and timing of systems ordered, shipped and recognized in revenue, risks relating to fluctuations in net bookings and our ability to convert bookings into sales, the risk of order cancellation or push outs and restrictions on shipments of ordered systems under export controls, ris s relating to technology, product and customer roadmaps and Mooreâ€™s law, risks relating to the trade environment, import/export and national security regulations and orders and their impact on us, including the impact of changes in export regulations and the impact of such regulations on our ability to obtain necessary licenses and to sell our systems and provide services to certain customers, exchange rate fluctuations, changes in tax rates, available liquidity and free cash flow and liquidity requirements, our ability to refinance our indebtedness, available cash and distributable reserves for, and other factors impacting, dividend payments and share repurchases, the number of shares that we repurchase under our share repurchase programs, our ability to enforce patents and protect intellectual property rights and the outcome of intellectual property disputes and litigation, our ability to meet ESG goals and execute our ESG strategy, other factors that may impact SMLâ€™s business or financial results including the risk that actual results may differ materially from the models, potential and opportunity we present for 2030 and other future periods, and other ris s indicated in the ris factors included in SMLâ€™s nnual Report on Form 20-F for the year ended December 31, 2023 and other filings with and submissions to the US Securities and Exchange Commission. These forward-looking statements are made only as of the date of this document. We undertake no obligation to update any forward-looking statements after the date of this report or to conform such statements to actual results or revised expectations, except as required by law. This document and related discussions contain statements relating to our approach to and interim progress on achieving certain energy efficiency and greenhouse gas emissions reduction targets, including our ambition to achieve greenhouse gas neutrality References to â€œgreenhouse gas neutralâ€ means remaining emissions, after SMLâ€™s efforts to reach its GHG emission reduction targets, compensated by the same amount of metric tons of carbon credits that are verified against recognised quality standards. Page 36November 14, 2024 Â Public THANK YOU Â EX-99.5 6 exhibit995.htm EX-99.5 exhibit995 Public Page 1 Herman Boom DUV products and business opportunity ASML Investor Day Veldhoven, The Netherlands November 14, 2024 Executive Vice President and Head of Business Line DUV Small Talk 2024 Exhibit 99.5 Â Public Page 2 â€¢ DUV is and will remain a workhorse for the industry. â€¢ We continue to support both our advanced and mainstream semiconductor customers with a portfolio of immersion systems that address the need for both overlay and higher productivity. â€¢ Our XT and NXT dry DUV portfolio continues to provide full flexibility to our customers in performance and deliver best cost of technology by building on commonality and operational efficiency. â€¢ We are extending our portfolio with an i-line wide-field scanner that provides the industryâ€™s highest productivity and solutions for advanced packaging applications. â€¢ We are optimizing our installed base of >6,000 systems by extending the product lifetime to >20 years and improving productivity with a diversified service and upgrades portfolio. Summary Â Public Page 3 DUV EUV While EUV has become the standard for most LOGIC and DRAM critical layers, all other layers are patterned using DUV technology November 14, 2024 Â Public DUV is and will remain a workhorse of the industry Page 4 >900 Million wafer exposures 2030 EUV KrF ArFi ArF i-line 525 Million wafer exposures 2024 EUV KrF ArFi ArF i-line ASML Market research: expectations of total exposure area worldwide November 14, 2024 Â Public Cloud infrastructure Edge computing Energy transition Automation Healthcare, medical tech Technological sovereignty Working, learning remotely Hyperconnectivity Electrification, smart mobility Agricultural innovation Smarter use of limited resources DUV is present in all markets and supports many applications ranging from advanced to mainstream market segments Page 5 I-Line Advanced segments Mainstream segments Advanced segments Mainstream segments 300 mm 300 mm 300 mm 300 mm 300 mm 200 mm 300 mm 300 mm 200 mm 150 mm 300 mm ArFi KrF ArF DRAM NAND MPU ANALOG POWER OPTICAL SENSORS NON - OPTICAL SENSORS LOGIC Mainstream LOGICSPECIALTY MEMORY ADVANCED PACKAGING EUV November 14, 2024 Â Public Page 6 2010 2011 2012 2013 2014 2015 2016 2017 2018 2019 2020 2021 2022 2023 2024 2030 Added wafer exposures1 2025-2030 ArFi ArF KrF i-line More layers All DUV wavelength segments are expected to grow in wafer exposures per year due to the growth in volume of wafers and higher litho spend W a fe r e x p o s u re s p e r y e a r More wafers November 14, 2024 1 based on an average layer stack Â Public The DUV strategy and product portfolio address a comprehensive set of value and cost drivers in the holistic lithography triangle Page 7 Resolution ProductivityAccuracyPatterning Yield Ã— Ã— Ã— â€¢ i-line â€¢ KrF â€¢ ArF â€¢ ArFi â€¢ EUV / ArFi â€¢ Overlay â€¢ Local CDU â€¢ EPE â€¢ System Throughput â€¢ System performance upgrades â€¢ Overall equipment efficiency â€¢ Patterning process control â€¢ Optical metrology â€¢ E-beam metrology â€¢ AI based control â€¢ Service cost â€¢ Utilities cost â€¢ Power roadmap â€¢ Re-use â€¢ Materials â€¢ >20 years system extendibility â€¢ Commonality â€¢ Configurability Operational cost Environmental costSystem cost Lifetime/ + 1 Ton CO2 = 200 EUR + = November 14, 2024 Â Public The DUV strategy and product portfolio address a comprehensive set of value and cost drivers in the holistic lithography triangle Page 8 Resolution ProductivityAccuracyPatterning Yield Ã— Ã— Ã— â€¢ i-line â€¢ KrF â€¢ ArF â€¢ ArFi â€¢ EUV / ArFi â€¢ Overlay â€¢ Local CDU â€¢ EPE â€¢ System Throughput â€¢ System performance upgrades â€¢ Overall equipment efficiency â€¢ Patterning process control â€¢ Optical metrology â€¢ E-beam metrology â€¢ AI based control â€¢ Service cost â€¢ Utilities cost â€¢ Power roadmap â€¢ Re-use â€¢ Materials â€¢ >20 years system extendibility â€¢ Commonality â€¢ Configurability Operational cost Environmental costSystem cost Lifetime/ + 1 Ton CO2 = 200 EUR + = November 14, 2024 Â Public DUV portfolio in place to capture the growth opportunities across markets Page 9 i-line KrF ArF ArFi NXT:2150i NXT:2100i NXT:2050i NXT:1980i NXT:1470 XT:1460 XT:260 XT:400 Advanced Markets Mainstream Markets NXT:870 XT platform NXT platform XT:860 XT:1060 November 14, 2024 Â Public DUV portfolio in place to capture the growth opportunities across markets Page 10 NXT platform Advanced Markets Mainstream Markets November 14, 2024 ArFi NXT:2150i NXT:2100i NXT:2050i NXT:1980i Â Public ASMLâ€™s immersion portfolio has grown to be the backbone of the industry by providing mid-critical and high-end immersion scanners Page 11 2012 In s ta ll e d i m m e rs io n w a fe r c a p a c it y NXT:1970i NXT:2000iNXT:1950i NXT:1980i NXT:2050i NXT:2100i NXT:2150i Immersion system releases Total installed immersion wafer capacity 2024 2024 2006 2007 2008 2009 2010 2011 20132012 2015 2016 2017 20182014 2019 2020 2021 2022 2023 2024 > 1 3 0 0 s y s te m s High-end: NXT:2xx0i Mid-critical: NXT:19xxi 92% of added wafer capacity installed by ASML November 14, 2024 Â Public â€¦ and we keep investing in immersion technology to enable customer roadmaps and reduce cost of ownership further November 14, 2024 Page 12 Improving overlay to enable overlay critical applications Improving productivity to reduce cost of ownership for our customers High-end Immersion NXT:2xx0i Mid Critical Immersion NXT:1980i Matched Machine Overlay in nm 1.5 nm 1.3 nm 1.0 nm 2020 NXT:2050i 2022 NXT:2100i 2024 NXT:2150i NEXT <1.0 nm 295 WpH 295 WpH 310 WpH >310 WpH Productivity in Wafers per Hour 2023 NXT:1980Fi NEXT 330 WpH >330 WpH 2.5 nm MMOMatched Machine Overlay in nm Productivity in Wafers per Hour Â Public 0 0.5 1 1.5 2 Our high-end immersion systems are adopted by customers and ramping up fast and reliably November 14, 2024 Page 13 >>100 high-end immersion systems installed Fast ramp to a stable production of 5000 wafers per day 5000 14 21 Days after install W a fe rs p e r d a y Matched Machine Overlay improvements to <1.3nm NXT:2100i â‰¤ 1.3 nm NXT:2050i â‰¤ 1.5 nm Fleet 2022 2023 2024 N X T :2 x x 0 i in s ta ll e d b a s e NXT:2000i â‰¤ 2.0 nm Â Public NXT:2150i supports tight overlay requirements incl NXT-NXE cross-matching Provides 1.0 nm matched machine overlay and on product overlay improvement Page 14 New reticle heating control Reducing impact of reticle heating on overlay Conditioned reticle library Faster conditioning and lower reticle-to-reticle temperature variation Alignment 12 colors 65 marks, small marks, combined layout Scanner metrology software Improved setup repro for overlay Optical sensors Improved camera & thermal conditioning Optical correction elements Improved lens and cross matching control Wafer table Improved overlay & lifetime improvements NXT:2100i NXT:2150i Throughput â‰¥295 WpH â‰¥310 WpH MMO1 â‰¤1.3 nm â‰¤1.0 nm EUV-DUV matching 1.7nm 1.5nm On Product Overlay â‰¤1.7 nm (DRAM) â‰¤1.5 nm (DRAM) 1 MMO: matched machine (or machine to machine) overlay First shipment end 2024 November 14, 2024 Page 14 Â Public Improved correction capability enables the patterning image to be manipulated locally on the wafer to correct post wafer bonding overlay fingerprints Page 15 50 nm 2.5 nm Metrology ARRAY CMOS Wafer bonder Massive metrology Litho scanner Wafer deformation directly after bonding Overlay error after litho correction Actuators November 14, 2024 Â Public DUV portfolio in place to capture the growth opportunities across markets Page 16 i-line KrF ArF ArFi NXT:2150i NXT:2100i NXT:2050i NXT:1980i NXT:1470 XT:1460 XT:260 XT:400 Advanced Markets Mainstream Markets NXT:870 XT platform NXT platform XT:860 XT:1060 November 14, 2024 Â Public DUV portfolio in place to capture the growth opportunities across markets Page 17 KrF XT platform NXT platform Advanced Markets Mainstream Markets NXT:870 XT:1060 XT:860 November 14, 2024 Â Public The NXT and XT platforms serve high-volume wafer fabs with different product mixes Page 18 Analog Power Mainstream Logic Advanced Packaging 300 mm 200 mm Various substrates Optical Sensors Specialty memory 300 mm DRAM NAND # of different products # r u n s p e r p ro d u c t # of different products # r u n s p e r p ro d u c t â€œA large number of products fill the fabâ€ â€œA couple of high-runner products fill the fabâ€ ustomer ab Tail: >1500 products Tail: <40 products ustomer ab Low-product-mix fabHigh-product-mix fab Typical in Mainstream segments Typical in Advanced segments Logic & MPU November 14, 2024 Â Public â€¦and will continue to serve new wafer fabs across the world November 14, 2024 Page 19 XT characteristics NXT characteristics Analog Power Mainstream Logic Advanced Packaging 300 mm 200 mm Various substrates Optical Sensors Specialty memory 300 mm DRAM NAND Logic & MPU Â Public The NXT:870 KrF scanner has seen a solid and rapid adoption with proven productivity and reliability based on the NXT platform Page 20 NXT:870 system installed base growing rapidly >5200 wafers per day in 13-weeks-average 7000 wafers per day Distribution wafers per day2022 2023 2024 Stable fleet production of >5200 wafers per day N X T :8 7 0 i n s ta ll e d b a s e Fleet up-time availability Fleet availability well above 95% at 13-weeks averaged 95% 100% November 14, 2024 13 weeks Â Public The NXT:870B KrF scanner will build on and extend the NXT platform to â‰¥400 WpH Page 21 Wafer Stage Reduced settling time, improved dynamics and productivity System Dynamics Improved wafer stage and base frame damping Wafer Handler Improved conditioning and higher productivity UV - Level Sensor 35 beams for productivity Reticle stage Faster scanning, shorter prep time Improved clamps Projection optics Improved lens with reduced lens heating and additional lens manipulators Reticle/Stage Align Improved alignment for productivity and performance XT:860N NXT:870 NXT:870B Throughput â‰¥260 WpH â‰¥330 WpH â‰¥400 WpH MMO1 â‰¤7.5 nm â‰¤6.0 nm â‰¤6.0 nm On Product Overlay2 â‰¤6.0 nm â‰¤5.0 nm â‰¤4.0 nm First shipment end 2024 November 14, 2024 1 Matched Machine Overlay, 2 For specific use-cases Page 21 Â Public DUV portfolio in place to capture the growth opportunities across markets Page 22 i-line KrF ArF ArFi NXT:2150i NXT:2100i NXT:2050i NXT:1980i NXT:1470 XT:1460 XT:260 XT:400 Advanced Markets Mainstream Markets NXT:870 XT platform NXT platform XT:860 XT:1060 November 14, 2024 Â Public DUV portfolio in place to capture the growth opportunities across markets Page 23 i-line XT platform Advanced Markets Mainstream Markets XT:260 XT:400 November 14, 2024 Â Public XT:260 delivers the highest productivity in the industry for advanced packaging applications which could benefit from a larger exposure field size Page 24 XT:260 large field exposure system supports high throughput for increasing interposer sizes Throughput of XT:260 Throughput of current 4x stepper/scanner 2x 350 WpH 150 WpH XT:260 large field system First shipment H2-2025 15 WpH 8x 4x 1x 1 2 3 4 5 6 7 8 Interposer size x (26 mm by 33 mm) 4x stepper field size (26x33mm) XT:260 2x scanner field size (52x68mm) November 14, 2024 1x 8x 4x 2x Â Public The DUV strategy and product portfolio address a comprehensive set of value and cost drivers in the holistic lithography triangle Page 25 Resolution ProductivityAccuracyPatterning Yield Ã— Ã— Ã— â€¢ i-line â€¢ KrF â€¢ ArF â€¢ ArFi â€¢ EUV / ArFi â€¢ Overlay â€¢ Local CDU â€¢ EPE â€¢ System Throughput â€¢ System performance upgrades â€¢ Overall equipment efficiency â€¢ Patterning process control â€¢ Optical metrology â€¢ E-beam metrology â€¢ AI based control â€¢ Service cost â€¢ Utilities cost â€¢ Power roadmap â€¢ Re-use â€¢ Materials â€¢ >20 years system extendibility â€¢ Commonality â€¢ Configurability Operational cost Environmental costSystem cost Lifetime/ + 1 Ton CO2 = 200 EUR + = November 14, 2024 Â Public Commonality in the NXT platform and between DUV and EUV gives shorter development lead time, more customer upgradability and lower operational cost November 14, 2024 Page 26 DUV NXT platform EUV NXE platform Level sensor Alignment sensor Metrology Wafer handling Common technology across DUV and EUV platforms Common technology across DUV wavelengths NXT:870 NXT:1470 NXT:2050iWafer stage Reticle stage Reticle handling Options KrF ArF ArFi Common technology within a wavelength NXT:870 NXT:870B Light source Sensors Optical modules KrF KrF Â Public Commonality is an important factor in driving efficiency across the value chain Cost effective way to increase factory output and reduce installation time Page 27 Pre-install before shipment system CUSTOMERASML Standard set up for building both XT and NXT systems Direct pre-shipment to customer November 14, 2024 Â Public Commonality is an important factor in driving efficiency across the value chain Cost effective way to increase factory output and reduce installation time Page 28 Pre- install before shipment system CUSTOMERASML Standard set up for building both XT and NXT systems Direct pre-shipment to customer November 14, 2024 Â Public Commonality is an important factor in driving efficiency across the value chain Cost effective way to increase factory output and reduce installation time Page 29 NXT Direct pre-shipment to customer Pre- install before shipment system CUSTOMERASML Standard set up for building both XT and NXT systems November 14, 2024 Â Public Commonality is an important factor in driving efficiency across the value chain Cost effective way to increase factory output and reduce installation time Page 30 NXTXT Pre- install before shipment system CUSTOMERASML Standard set up for building both XT and NXT systems Direct pre-shipment to customer November 14, 2024 Â Public Commonality is an important factor in driving efficiency across the value chain Customer Page 31 Commonality benefits November 14, 2024 Â Public With commonality we reduce cost, development lead times, cycle times, have lower inventory, faster ramp-up, improve upgradability and re-use To customer Lower Cost Innovation Higher Quality Page 32 FactorySupply chain Install ServiceD&E Commonality Benefits Reduced cycle timeReduced design cost Faster installation Faster ramp-up Upgradability Lower inventory Lower parts cost Lower OPEX More repair and re-use Higher availability November 14, 2024 Â Public Along with product design, operational innovation is applied to reduce cost and the environmental footprint of our operations Page 33November 14, 2024 Â Public ASML has shipped >6000 systems to its customers since we started our operations Page 34 1985 1990 1995 2005 20252010 2015 20202000 2030 10,000 9000 8000 7000 6000 5000 4000 3000 2000 1000 0 EUV ArFi ArF KrF i-line ASML installed base Numbers of systems in the field November 14, 2024 Â Public Continued focus on the upgrade and service portfolio to maintain and improve the performance as well as the cost effectiveness of the installed base V a lu e [a .u .] 0 10yrs 20yrs Page 35 Regular service warranty NXT-platform XT-platform PAS-platform AT-platform EXTEND installed base IMPROVE installed base Extended Service Value-up Service (Field) Upgrades Portfolio expansion Refresh Trade-in / buy-back November 14, 2024 Refresh Â Public Our market opportunity of our growing installed based with an expanding service & upgrade portfolio November 14, 2024 Page 36 Regular service Value-up service Extended service Field Upgrades Installed base growth Trade-in & Refurb 0.0x 1.0x 2.0x 3.0x 4.0x 5.0x 2019 2020 2021 2022 2023 2024 2025 2026 2027 2028 2029 2030 Regular service revenue Value-up service revenue Regular life Services Extended life Services Â Public November 14, 2024 Page 37 Our NXT immersion (Field) upgrades enable improved on-product performance and higher wafer output Matched Machine Overlay 5.5 nm 3.5 nm 2.5 nm 2.0 nm 1.5 nm 1.3 nm 4.5 nm 4.0 nm 1.0 nm NXT:1960Bi NXT:1980Di NXT:2050i NXT:2100i NXT:1980Ei NXT:1980Fi NXT:1965Ci NXT:1970Ci NXT:2000i NXT:2150i Productivity Package Wafer per day package Node Enhancement Package Development NXT:1950i 190 WPH 230 WPH 250 WPH 275 WPH 295 WPH 310 WPH 330 WPH System NXT:2000Ei Â Public â€¢ DUV is and will remain a workhorse for the industry. â€¢ We continue to support both our advanced and mainstream semiconductor customers with a portfolio of immersion systems that address the need for both overlay and higher productivity. â€¢ Our XT and NXT dry DUV portfolio continues to provide full flexibility to our customers in performance and deliver best cost of technology by building on commonality and operational efficiency. â€¢ We are extending our portfolio with an i-line wide-field scanner that provides the industryâ€™s highest productivity and solutions for advanced packaging applications. â€¢ We are optimizing our installed base of >6,000 systems by extending the product lifetime to >20 years and improving productivity with a diversified service and upgrades portfolio. Summary Page 38 Â Public Forward Looking Statements This document and related discussions contain statements that are forward-looking within the meaning of the U.S. Private Securities Litigation Reform Act of 1995, including statements with respect to our strategy, plans and expected trends, including trends in end markets and the technology industry and business environment trends, including the emergence of AI and its potential opportunities and expectations for the semiconductor industry, including computing power, advanced logic nodes and DR M memory, statements with respect to Mooreâ€™s law and expected transistor growth and aspirations by 2030, global market trends and technology, product and customer roadmaps, long term outlook and expected lithography and semiconductor industry growth and trends and expected growth in semiconductor sales and semiconductor market opportunity through to 2030 and beyond, expected growth in wafer demand and capacity and additional wafer capacity requirements, expected investments by our customers, including investments in our technology and in wafer capacity, plans to increase capacity, expected growth in lithography spend, growth opportunities including opportunities for growth in service and upgrades and opportunities for growth in Installed Base Management sales, expected growth and gross margins in the holistic lithography business and expected addressable market for pplications products, expectations and benefits of a growing installed base, SMLâ€™s and its supplierâ€™s capacity, expected production of systems, model scenarios and the updated model for 2030, including annual revenue and gross margin opportunity and development potential for 2030, outlook and expected, modelled or potential financial results, including revenue opportunity, gross margin, R&D costs, SG&A costs, capital expenditure, cash conversion cycle and annualized effective tax rate for 2030 and assumptions and drivers underlying such expected, modelled or potential amounts, and other assumptions underlying our business and financial models, expected trends, outlook and growth in semiconductor end markets and long term growth opportunities, demand and demand drivers, expected opportunities and growth drivers for and technological innovation of our products including DUV EUV, High NA, Hyper NA, Applications, and other products impacting productivity and costs, transistor dimensions, logic and DRAM shrink, foundry competition, statements with respect to dividends and share buybacks and our capital return policy, including expectation to return significant amounts of cash to shareholders through growing dividends and buybacks and statements with respect to energy generation and consumption trends and the drive toward energy efficiency, emissions reduction and greenhouse gas neutrality goals and target dates to achieve greenhouse gas neutrality, zero waste from operations and other ESG targets and ambitions and plans to maintain a leadership position in ESG, increasing technological sovereignty across the world and the expected impact on semiconductor sales, including specific goals of countries across the world, increasing competition in the foundry business, estimates for 2024 and other non-historical statements. You can generally identify these statements by the use of words like "may", "will", "could", "should", "project", "believe", "anticipate", "expect", "plan", "estimate", "forecast", "potential", â€œopportunityâ€, â€œscenarioâ€, â€œguidance,â€ "intend", "continue", "target", "future", "progress", "goal" and variations of these words or comparable words. These statements are not historical facts, but rather are based on current expectations, estimates, assumptions, models, opportunities and projections about our business and our future and potential financial results and readers should not place undue reliance on them. Forward- looking statements do not guarantee future performance and involve a number of substantial known and unknown risks and uncertainties. These risks and uncertainties include, without limitation, customer demand, semiconductor equipment industry capacity, worldwide demand for semiconductors and semiconductor manufacturing capacity, lithography tool utilization and semiconductor inventory levels, general trends and consumer confidence in the semiconductor industry and end markets, the impact of general economic conditions, including the impact of the current macroeconomic environment on the semiconductor industry, uncertainty around a market recovery including the timing thereof, the impact of inflation, interest rates, wars and geopolitical developments, the impact of pandemics, the performance of our systems, the success of technology advances and the pace of new product development and customer acceptance of and demand for new products, our production capacity and ability to adjust capacity to meet demand, supply chain capacity, timely availability of parts and components, raw materials, critical manufacturing equipment and qualified employees, our ability to produce systems to meet demand, the number and timing of systems ordered, shipped and recognized in revenue, risks relating to fluctuations in net bookings and our ability to convert bookings into sales, the risk of order cancellation or push outs and restrictions on shipments of ordered systems under export controls, risks relating to technology, product and customer roadmaps and Mooreâ€™s law, risks relating to the trade environment, import/export and national security regulations and orders and their impact on us, including the impact of changes in export regulations and the impact of such regulations on our ability to obtain necessary licenses and to sell our systems and provide services to certain customers, exchange rate fluctuations, changes in tax rates, available liquidity and free cash flow and liquidity requirements, our ability to refinance our indebtedness, available cash and distributable reserves for, and other factors impacting, dividend payments and share repurchases, the number of shares that we repurchase under our share repurchase programs, our ability to enforce patents and protect intellectual property rights and the outcome of intellectual property disputes and litigation, our ability to meet ESG goals and execute our ESG strategy, other factors that may impact SMLâ€™s business or financial results including the risk that actual results may differ materially from the models, potential and opportunity we present for 2030 and other future periods, and other risks indicated in the risk factors included in SMLâ€™s nnual Report on Form 20-F for the year ended December 31, 2023 and other filings with and submissions to the US Securities and Exchange Commission. These forward-looking statements are made only as of the date of this document. We undertake no obligation to update any forward-looking statements after the date of this report or to conform such statements to actual results or revised expectations, except as required by law. This document and related discussions contain statements relating to our approach to and interim progress on achieving certain energy efficiency and greenhouse gas emissions reduction targets, including our ambition to achieve greenhouse gas neutrality. References to â€œgreenhouse gas neutralâ€ means remaining emissions, after SMLâ€™s efforts to reach its GHG emission reduction targets, compensated by the same amount of metric tons of carbon credits that are verified against recognised quality standards. Page 39November 14, 2024 Â Public THANK YOU Page 40 Â EX-99.6 7 exhibit996.htm EX-99.6 exhibit996 Public Marco Pieters ASML Investor Day Veldhoven, The Netherlands November 14, 2024 Executive Vice President and Head of Business Line Applications Small Talk 2024 Holistic Lithography Solutions and business opportunity Exhibit 99.6 Â Public Holistic Lithography Opportunity & Growth Drivers â€¢ Holistic Lithography focuses on improving Accuracy and Patterning Yield for our customers. â€¢ Accuracy: drive improvements in Overlay and Edge Placement Error (EPE) via Computational Lithography (physical models & AI), Metrology & Inspection and Scanner Optimization. â€¢ Patterning Yield: drive cost effective metrology and inspection solutions for both 2D and 3D structures enabling early yield ramp and holistic lithography control â€¢ Significant progress on multi e-beam inspection and the opportunity for HVM, first application will be Voltage Contrast inspection â€¢ Followed by smaller 2D features and 3D structures requiring buried defect inspection â€¢ Enable front end 3D integration (wafer bonding) with metrology and control solutions to meet customer overlay requirements. â€¢ The Holistic Lithography business is expected to grow at >15% CAGR with strong gross margins from 2025 to 2030. Computational lithography and metrology Metrology and inspection Lithography scanner with advanced control capability EUV DUV Â Public â€¢ Patterning process control â€¢ Optical metrology â€¢ E-beam metrology â€¢ E-beam inspection â€¢ AI based models â€¢ Overlay â€¢ Local CDU â€¢ Edge Placement Error (EPE) Holistic lithography enables our customers to maximize Good Wafers per Day Our product portfolio focuses on Patterning Yield and Accuracy Resolution ProductivityÃ— Ã— Ã— â€¢ Advanced ArFi â€¢ EUV 0.33 NA â€¢ EUV 0.55 NA â€¢ System Throughput â€¢ Overall equipment efficiency Operational cost Environmental costSystem cost Lifetime/ + 1 Ton CO2 = 200 EUR + = Patterning Yield Accuracy Page 3November 14, 2024 Â EPE: Edge Placement Error Source: 1Luc van den Hove, IMEC , ITF May 21, 2024 0 5 10 15 30 20 25 21 18 16 14 28 4,3 3,5 3,5 Public data Customer projection 2020 2023 2025 2027 2029 2031 2033 2035 17 14 3,8 22 23 E P E [n m], N o d e , m e t a l p i t c h , L in e a r s c a le Year of high-volume production 7 20392037 12 3 5 3 2 1,4 1,0 0,7 0,20,5 0,3 sub-0.2 Logic metal pitch [nm] Edge placement error [nm] Uncertainty 5,5 4,5 5,8 Node name1 [nm] 40 Estimate Public Page 4 0 50 200 100 150 B a c k -s id e M e t a l P it c h e s ti m a te [n m] range backside metal pitch 165 65 115 45 42 40 34 40 28 90 5,2 Logic roadmap continues to drive shrink, requires improvements in Edge Placement Errors, tightens backside metal pitch and post bonding overlay November 14, 2024 Â Public Evolving Industry Roadmap drives growth opportunity for Applications Products Patterning Yield Accuracy DRIVERS TRENDS Computational Lithography Litho & Etch Model accuracy, Compute cost Physical models â†’ + Deep learning Rectangular â†’ Freeform mask patterns CPU â†’ Hybrid/GPU compute Scanner and Process Control Software Transition to EPE, Pitch shrink, Wafer bonding overlay solutions Overlay, CD â†’ EPE HVM: DUV â†’ DUV + EUV â†’ HNA EUV Low â†’ Higher order scanner corrections Page 5November 14, 2024 High Resolution Inspection Resolution & Throughput Electrical and Buried defects Single Beam / Optical â†’ Multibeam (incl Voltage Contrast) Optical and E-beam Metrology Accuracy, Precision, Local stochastic effects Optical Overlay: â€¢ Targets â†’ Device â€¢ More sampling E-beam: â€¢ Small â†’ Large field â€¢ Massive metrology Â Public Evolving Industry Roadmap drives growth opportunity for Applications Products Page 6 2023 2026 2030 Scanner and Process Control Software Computational Lithography Optical and E-beam Metrology High Resolution Inspection (optical & E-beam) 5.4 Bâ‚¬ 7.6 Bâ‚¬ 11 Bâ‚¬ Total Addressable Market EUV DUV Metrology and inspection November 14, 2024 Computational lithography and metrology Â Public Lithography is a formidable tool to compensate process fingerprints Correction capability increased ~5 orders of magnitude Exposure stage 100% of wafers are measured 100% of wafers are processed field-by-field Metrology stage Even Fingers Odd Fingers Grey Filter X Y Z Optical Centerline Dose manipulator Flexible Illuminator Reticle stage 1975 1980 1985 1990 1995 2000 2005 2010 2015 2020 2025 1000 100 10 1 0.1 O v e rl a y [n m] Page 7 1,000 100 10 1 10,000 # u s e r s e le c ta b le l it h o c o rr e c ti n o s p e r lo t 100,000 Increasing correction capability per field, wafer, lot Scanner and Process Control SoftwareScanner and Process Control Software November 14, 2024 Â Public Holistic approach improved overlay ~3 orders of magnitudeâ€‹ Correction capability increased ~5 orders of magnitude and overlay improved ~3 orders of magnitude Exposure stage 100% of wafers are measured 100% of wafers are processed field-by-field Metrology stage Even Fingers Odd Fingers Grey Filter X Y Z Optical Centerline Dose manipulator Flexible Illuminator Reticle stage 1975 1980 1985 1990 1995 2000 2005 2010 2015 2020 2025 1000 100 10 1 0.1 Overlay achieved lithography O v e rl a y [n m] Page 8 # of parameters available for control with holistic lithography Growing importance of holistic Lithography Overlay achieved with holistic Litho 1,000 100 10 1 10,000 100,000 Scanner and Process Control Software November 14, 2024 # u s e r s e le c ta b le l it h o c o rr e c ti n o s p e r lo t Â Public # u s e r s e le c ta b le l it h o c o rr e c ti n o s p e r lo t Holistic approach improved overlay ~3 orders of magnitude and extending to EPE gives another opportunity to improve Yieldâ€‹ 1975 1980 1985 1990 1995 2000 2005 2010 2015 2020 2025 1000 100 10 1 0.1 Overlay achieved lithography O v e rl a y [n m] Page 9 # of parameters available for control with holistic lithography Growing importance of holistic Lithography Overlay achieved with holistic Litho 1,000 100 10 1 10,000 100,000 Correlation to yield EPE OVL CD Scanner and Process Control SoftwareScanner and Process Control Software November 14, 2024 Â Public DUV EUV insertion High-NA EUV insertion Page 10 2010 2012 2014 2020 2022 2024 2026 2028 2030 10000 1 2016 2018 100 10 1000 Metrology # Parameters in model # of metrology gauges Physical models + Metrology + AIPhysical Models Accuracy Cost Ai Computational Lithography Computational litho: optical proximity correction accuracy has improved rapidly thanks to the introduction of machine learning and massive metrology a .u . November 14, 2024 Â Public Optimizing Patterning Yield by combining metrology data and translating this to scanner actuations Page 11 patterning (Layer N+1) overlay metrology e-beam metrology e-beam metrology patterning (Layer N) global CD Layer N Layer N and Layer N+1 overlay Layer N+1 global CD local CDU & placementline edge roughness =+ + + + Dose and grid actuations to minimize EPE Low/medium density e-beam Low/medium density e-beam High density e-beam High density e-beam Optical or e-beam Edge Placement Errors Computational Lithography (Optical Proximity Correction) EPE-aware optimization leverages all information from dense metrology Data by courtesy of Tae Kwon Jee, SK Hynix Inc. S u : H ASML, S I , â€œTh p h z p z RAM n sâ€ November 14, 2024 Â Public Massive overlay metrology is needed to drive those scanner corrections YieldStar platform enables increase of sampling by 80% while cost effectiveness is improved by 30~45% every 4 years Page 12 100% 90% 80% 70% 60% 50% 40% 30% 20% 0% 14000 13000 12000 11000 10000 9000 8000 7000 6000 5000 4000 3000 2000 1000 0 2010 2014 2018 2022 2026 2030 M e t r o lo g y c o s t p e r p o in t P o in ts m e a s u re d p e r lo t 40% 20% 40% 45% 800 1400 2400 5200 7000 14000 Opportunity driven by tighter resolution and wafer bonding requirement of >2000 point per wafer. Optical and E-beam Metrology 30% November 14, 2024 Â Public YieldStar installed base reached >1000 systems in H1â€™24 Page 13 Optical and E-beam Metrology 2010 2015 2020 2024 1200 1000 800 600 400 200 0 N u m b e r o f s h ip m e n ts [c u m u la ti v e] â€™23â€™22â€™21â€™19â€™18â€™17â€™16â€™14â€™13â€™12â€™11â€™09â€™08 November 14, 2024 Â Public Patterning Yield: e-beam opportunity for physical, buried defects and voltage contrast Voltage contrast is driving the insertion of e-beam inspection in High Volume Manufacturing Page 14 160 1040 20 8 6 4 2 Defect size [nm] Buried and electric defects Extra high resolution physical inspection of buried defects (high landing energy) VC inspection and See-through (e-beam only) * Source: Tuyen Tran, Metrology and Diagnostic Techniques for Nanoelectronics, 1st edition, 2016, ISBN-10: 9814745081 <10nm defects Extra high resolution physical inspection of surface defects (low landing energy) Physical inspection (e-beam only) >10nm defects Medium resolution physical inspection for inline monitoring Physical inspection (mainly optical) High resolution physical inspection for inline monitoring Progress has been made in optical inspection, but new node development requires higher resolution to capture defects well below 10nm More complex 3D structures fuel the need for Voltage Contrast Inspection, started with NAND, moving now to DRAM and Logic â€œâ€¦ h s s w detected by any optical inspection tool, ss sp â€* Voltage contrast inspection on-product monitoring November 14, 2024 Â Public Voltage contrast inspection adopted in NAND HVM, expanding to Logic and DRAM Unique capability of electron beam inspection to find yield limiting defects Page 15 100 % 0 % 0 5 10 15 20 25 3530 EPE [nm] E-beam Voltage Contrast measurements confirm that EPE is a proxy for yield M e a s u r e d b it y ie ld b y V o lt a g e C o n tr a s t VC inspection: detection of interlayer defects causing electric opens and shorts Heavily used in 3D NAND Expanding usage in DRAM and Logic Voltage Contrast Inspection Installed Systems (2019-2023) 10% 90% November 14, 2024 Â Public Multibeam eScan 1100, larger wafer coverage and better CoO, enabled by >10x throughput >10 eScan1100 systems at >5 customers for evaluation and qualification for Voltage Contrast in HVM â€¢ Demonstrated value in customer evaluations: larger wafer coverage capable of capturing wafer defect fingerprints for inline monitoring, enabled by faster throughput and lower cost of ownership >10x higher throughput compared to single beam on logic and DRAM layers Limited die sampling unable to catch wafer defect signature 100% die sampling captures clear wafer defect fingerprint single beam eScan1100 (multi beam) 0.1 - 0.2% coverage 1 - 2% coverage 100 10 1 A B C D E F G H I J K L M N O T h ro u g h p u t ra tio e S c a n 1 1 0 0 v s s in g le b e a m DRAMLOGIC eScan1100 TPut upgrade Q1â€™25 (every bar is a layer) Page 16November 14, 2024 Â Public Customer data shows eScan1100 capturing clear defect signature with higher throughput 7~8x larger wafer coverage and ~60% shorter cycle time * based on full wafer area size as 707cmÂ² Page 17 Single Beam Inspection eScan1100 Wafer coverage: 0.2% Wafer coverage: 1.5%* Inspection time: 100% Inspection time: ~40% Miss the signature Clear defect signature November 14, 2024 Â Public Multibeam enables higher throughput and larger wafer coverage in voltage contrast and physical inspection for inline defect monitoring in HVM Page 18 2019 2020 2021 2023 2024 2025 2026 2027 2028 2029 100 1000 10 1N o rm a li z e d t h r o u g h p u t (L o g i c a n d D R A M) 100% wafer area per hour (VC inspection) eScan 430 Escan 600 eScan 460 eP5 XLE eScan 4x0 Next eP7 XLE HVM adoption (Physical inspection) 2022 2030 eScan 1100 Generation 1 Generation 2 Generation 3 eScan 2200 NEXT HVM: High Volume manufacturing | VC: Voltage Contrast HVM adoption (VC inspection) November 14, 2024 Â Public Next step in multibeam: from 25 to >2700 beams Technology demonstration ongoing, working towards customer early access in 2025 Focal plane verification Through focus measurement >2700 beams on scintillator screen All of >2700 beams on scintillator screen are functional Detector functionality and resolution verification Sample image Page 19November 14, 2024 Â Public We expect front end 3D integration to complement 2D shrink in driving density Front end 3D integration challenges will trigger new litho opportunities for all semiconductor products Page 20 Stack LOGIC W-W hybrid W-W Fusion W-W | D-W Fusion Overlay 3D NAND BSPN CFET HVM 2026 >2032 Array CMOS Logic Bare-Si Logic Logic Bonding 5nm â†’ 2nm50nm â†’ 25nm 2.5nm â†’ 1.6nm Litho KrF NXE/EXE NXE/EXE Array W-W / D-W hybrid Array CMOS 50nm â†’ 25nm KrF NAND DRAM W-W hybrid W-W hybrid W-W / D-W hybrid 3D ARRAY4F2 2D ARRAY >2027 >2032 >2032 Array CMOS Array CMOS Array CMOS Array >4.5nm6nm â†’ 3nm 6nm â†’ 3nm ArFiArFi ArFi >2030 November 14, 2024 Â Public Holistic Lithography will enable 3D integration Metrology and scanner control at pre and post bonding critical process points needed for overlay Page 21 < 5 nm overlay error Both wafers have separate patterning and processes but overlay needs to be matched between them prior to bonding Pre-bonding ARRAY CMOS Bonder creates a massive deformation on the wafer CMOS Scanner correction and control2 ARRAY Scanner and offline metrology1 Actuators Bonding November 14, 2024 Â Public Holistic Lithography will enable 3D integration Metrology and scanner control at pre and post bonding critical process points needed for overlay Page 22 Actuators Holistically bringing the overlay after bonding back to customer requirements Post-bonding >2000 measurements/wafer <

5 nm overlay error 3 Bonder creates a massive deformation on the wafer Bonding >5000 measurements/wafer >50nm overlay error Standard bonding recipe, optimizing post bonding grid Co-optimized bonding recipe, optimizing post bonding litho Wafer deformation directly after bonding Overlay error after litho correction Wafer deformation directly after bonding Overlay error after litho correctionRequires massive metrology on every wafer to categorize the large (local) variety in fingerprint Richard van Haren, at all, ASML, EVG, Leti:, â€œCharacterization and mitigation of local wafer deformations introduced by direct wafer-to-wafer bondingâ€, SPIE Advanced Lithography + Patterning, 2024 November 14, 2024 Â Public Holistic Lithography will enable 3D integration Metrology and scanner control at pre and post bonding critical process points needed for overlay Page 23 Pre-bonding CMOS Scanner correction and control ARRAY Scanner and offline metrology 2 1 Actuators Post-bondingBonding ARRAY CMOS massive metrology Actuators large wafer deformation 3 Metrology Litho scanner Holistic lithography process control points Actuators 321 >5000 measurements/wafer 50~100nm overlay error >2000 measurements/wafer < 5 nm overlay error< 5 nm overlay error Holistic lithography to bring overlay error within spec November 14, 2024 Â Public Holistic Lithography Opportunity & Growth Drivers â€¢ Holistic Lithography focuses on improving Accuracy and Patterning Yield for our customers. â€¢ Accuracy: drive improvements in Overlay and Edge Placement Error (EPE) via Computational Lithography (physical models & AI), Metrology & Inspection and Scanner Optimization. â€¢ Patterning Yield: drive cost effective metrology and inspection solutions for both 2D and 3D structures enabling early yield ramp and holistic lithography control â€¢ Significant progress on multi e-beam inspection and the opportunity for HVM, first application will be Voltage Contrast inspection â€¢ Followed by smaller 2D features and 3D structures requiring buried defect inspection â€¢ Enable front end 3D integration (wafer bonding) with metrology and control solutions to meet customer overlay requirements. â€¢ The Holistic Lithography business is expected to grow at >15% CAGR with strong gross margins from 2025 to 2030. Computational lithography and metrology Metrology and inspection Lithography scanner with advanced control capability EUV DUV Â Public Forward Looking Statements This document and related discussions contain statements that are forward-looking within the meaning of the U.S. Private Securities Litigation Reform Act of 1995, including statements with respect to our strategy, plans and expected trends, including trends in end markets and the technology industry and business environment trends, including the emergence of AI and its potential opportunities and expectations for the semiconductor industry, including pu p w , s RAM , s s w h sp M â€™s w xp s s w h and aspirations by 2030, global market trends and technology, product and customer roadmaps, long term outlook and expected lithography and semiconductor industry growth and trends and expected growth in semiconductor sales and semiconductor market opportunity through to 2030 and beyond, expected growth in wafer demand and capacity and additional wafer capacity requirements, expected investments by our customers, including investments in our technology and in wafer capacity, plans to increase capacity, expected growth in lithography spend, growth opportunities including opportunities for growth in service and upgrades and opportunities for growth in Installed Base Management sales, expected growth and gross margins in the holistic lithography business and xp ss b k App s p u s, xp s b s w s b s , ASMLâ€™s s supp â€™s p , xp p u s s s, s s h up 2030, including annual revenue and gross margin opportunity and development potential for 2030, outlook and expected, modelled or potential financial results, including revenue opportunity, gross margin, R&D costs, SG&A costs, capital expenditure, cash conversion cycle and annualized effective tax rate for 2030 and assumptions and drivers underlying such expected, modelled or potential amounts, and other assumptions underlying our business and financial models, expected trends, outlook and growth in semiconductor end markets and long term growth opportunities, demand and demand drivers, expected opportunities and growth drivers for and technological innovation of our products including DUV EUV, High NA, Hyper NA, Applications, and other products impacting productivity and costs, transistor dimensions, logic and DRAM shrink, foundry competition, statements with respect to dividends and share buybacks and our capital return policy, including expectation to return significant amounts of cash to shareholders through growing dividends and buybacks and statements with respect to energy generation and consumption trends and the drive toward energy efficiency, emissions reduction and greenhouse gas neutrality goals and target dates to achieve greenhouse gas neutrality, zero waste from operations and other ESG targets and ambitions and plans to maintain a leadership position in ESG, increasing technological sovereignty across the world and the expected impact on semiconductor sales, including specific goals of countries across the world, increasing competition in the foundry business, estimates for 2024 and other non-historical statements. You can generally identify these statements by the use of words like "may", "will", "could", "should", "project", "believe", "anticipate", "expect", "plan", " s ", " s ", "p ", â€œ pp u â€, â€œs â€, â€œ u ,â€ " ", " u ", " ", " u u ", "p ss", "goal" and variations of these words or comparable words. These statements are not historical facts, but rather are based on current expectations, estimates, assumptions, models, opportunities and projections about our business and our future and potential financial results and readers should not place undue reliance on them. Forward- looking statements do not guarantee future performance and involve a number of substantial known and unknown risks and uncertainties. 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These forward-looking statements are made only as of the date of this document. We undertake no obligation to update any forward-looking statements after the date of this report or to conform such statements to actual results or revised expectations, except as required by law. This document and related discussions contain statements relating to our approach to and interim progress on achieving certain energy efficiency and greenhouse gas emissions reduction targets, including our ambition to achieve h us s u . R s â€œ h us s u â€ s ss s, ASMLâ€™s s h s GHG emission reduction targets, compensated by the same amount of metric tons of carbon credits that are verified against recognised quality standards. Page 25November 14, 2024 Â Public THANK YOU Â EX-99.7 8 exhibit997.htm EX-99.7 exhibit997 Public November 14, 2024 Roger Dassen Business model and capital allocation strategy ASML Investor Day Veldhoven, The Netherlands November 14, 2024 Chief Financial Officer Small Talk 2024 Exhibit 99.7 Â Public Business model and capital allocation strategy Our continued investments in technology leadership have created significant shareholder value. Investments create value We expect substantial growth opportunities in this decade Based on different market and technology scenarios, we see an opportunity to achieve the following by 2030: â€¢ Annual revenue between approximately â,¬44 billion and â,¬60 billion with gross margin between approximately 56% and 60% Market and technology opportunity Expected growth in semiconductor end markets and increasing lithography spending on future nodes fuel demand for our products and services. Growth in markets We confirm our financing policy; a solid capital and liquidity structure, based on which we will continue to invest in our business and expect to return significant amounts of cash to our shareholders through growing dividends and share buybacks. Capital allocation and financing Key messages November 14, 2024 Â Public November 14, 2024 Page 5 Continuing growth Continued shareholder value creation Historical shareholder value creation Â Public ASMLâ€™s technology leadership comes from strategic investments that enable cost-effective innovations for our customers Organic growth through investments in R&D and Capex Strategic acquisitions and investments in â€¢ Supply chain for technology and capacity (Carl Zeiss SMT, Berliner Glas) â€¢ New business (HMI) Page 6 * ASML contribution Zeiss SMT Capex included as of 2017 ** 2024E is estimate for the FY2024 figures Growth methods R&D Capex Investments 2014 2015 2016 2017* 2018 2019 2020 2021 2022 2023 2024E** 1,1 1,1 1,1 1,3 1,6 2,0 2,2 2,5 3,3 4,0 4,3 0,4 0,4 0,3 0,4 0,6 0,9 1,0 0,9 1,3 2,2 1,9 1,4 1,4 1,4 1,6 2,2 2,9 3,2 3,5 4,6 6,2 6,2 Berliner Glas acquisition Carl Zeiss SMT Holding acquisition 24.9% interest HMI acquisition â,¬ b n (â,¬1.0bn) (â,¬2.8bn) (â,¬0.3bn) November 14, 2024 Â Public ASMLâ€™s EPS has grown at a CAGR of 22% since 2014 driven by revenue growth, improved margins and share buybacks Page 7 Systems (â,¬bn) Gross margin (%)Installed Base Management (â,¬bn) EPS (â,¬) â€¢ Systems revenue grew at a 18% CAGR since 2014 â€¢ Installed Base Management* grew at a 14% CAGR since 2014 driven by upgrades and service of growing installed base â€¢ Gross margin improved from 44% in 2014 to over 50%, primarily as a result of progress in the EUV profitability while maintaining strong margins in the rest of the business â€¢ Earnings per share (EPS) grew at 22% CAGR since 2014 driven by profitability and share buyback * Installed Base Management equals our net service and field option sales ** 2024E is the midpoint guidance for FY24 Growth drivers 2014 2015 2016 2017 2018 2019 2020 2021 2022 2023 2024E** 4.2 4.2 4.6 6.4 1.6 2.1 2.2 2.75.9 6.3 6.8 9.1 10.9 2.7 8.3 11.8 2.8 10.3 3.7 9.0 14.0 18.6 5.0 13.7 15.4 5.7 21.2 5.6 27.6 28.0 21.9 6.2 21.8 14.14 2.74 3.22 3.46 4.93 6.10 6.16 8.49 14.36 19.91 44% 46% 45% 45% 46% 45% 49% 53% 51% 51% 51% Revenue/Gross margin/EPS November 14, 2024 Â Public ASML created significant shareholder value over the period 2010-2024* Page 8 Total Shareholder Return (TSR) annualized compounded : â€¢ ASML (Nasdaq) : 23% â€¢ Semiconductor index - SOX 22% â€¢ Technology index - Nasdaq 17% Source: Bloomberg (Total Shareholder Return: index = 2010) Total Shareholder Return (TSR) = share price increase + dividend pay-out 2024*: the graph includes data until November 6, 2024 2014 2015 2016 2017 2018 2019 2020 2021 2022 2023 2024* ASML (Nasdaq) NASDAQ S&P 500 SOX AEX Total Shareholder Return 1,500 1,000 500 0 3,000 2,500 2,000 3,500 4,000 2010 2011 2012 2013 November 14, 2024 Â Public November 14, 2024 Page 9 Continued shareholder value creation Historical shareholder value creation Continuing growth Â Public Page 10 Estimate growth of our Installed Base business Installed Base Management Model assumptions Start with end markets Translate to worldwide litho spending, convert to ASML share Litho spend Convert to wafer demand: High â€“ Moderate â€“ Low scenarios Wafer demandEnd markets Scenarios â†'High â†' Moderate â†' Low 2030 Model scenarios November 14, 2024 Â Public Semi sales expected to grow at 9% CAGR (2025-2030) & surpass $1tn by 2030 Sharp increase in growth for Servers, Datacenters & Storage offsets most of moderation elsewhere Page 11 Smartphone ($bn) Wired & wireless Infrastructure ($bn)

Automotive ($bn) Personal Computing ($bn) Servers, Datacenters & Storage ($bn) Industrial Electronics ($bn) Consumer Electronics ($bn) Total Semiconductor ($bn) 149 158 157 162 177 192 25 26 27 28 29 30 CMD 2022 CMD 2024 5% 92 100 100 101 106 112 25 26 27 28 29 30 4% 53 57 60 63 66 70 25 26 27 28 29 30 6% 70 72 74 78 80 83 25 26 27 28 29 30 3% 76 84 93 98 105 114 25 26 27 28 29 30 9% 84 91 98 100 110 120 25 26 27 28 29 30 7% 679 749 791 845 941 1051 25 26 27 28 29 30 9% 156 188 211 243 296 361 25 26 27 28 29 30 18% CMD 2022 CMD 2024 CMD 2022 CMD 2024 CMD 2022 CMD 2024 CMD 2022 CMD 2024 CMD 2022 CMD 2024 CMD 2022 CMD 2024 CMD 2022 CMD 2024 CMD 2022 CMD 2024 November 14, 2024 Source: ASML analysis Â Public Wafer capacity will be driven by both wafer demand & strategic considerations As a result, we expect 5-8% extra overall capacity by 2030 on top of demand-driven additions Page 12 â€¢ Tech sovereignty leading to less efficient use of the installed capacity as countries/regions aim to (re)gain fab footprint. â€¢ Increased emphasis on supply security resulting in geographically diversified ownership profile, in turn making load balancing more difficult. â€¢ Intensified competition could lead to period with overcapacity as players try to capture market share. Strategic considerationsWafer capacity: Million wafer starts/month (Mwspm) 11.2 15.1 2025 2030 5% 5-8% Growth 2025-2030 (Kwspm/yr.) Total wafer demand 780 Strategic considerations 85 Total wafer capacity 865 November 14, 2024 Source: ASML analysis Â Public Advanced logic & DRAM shrink is expected to drive further layers & spending Increase in exposures, combined with wafer volume translates into double-digit EUV spending CAGRs Page 13 Advanced Logic: Average # of Total EUV Exposures* EUV litho spending CAGR (2025-2030): 10-20% November 14, 2024 ; * Source: ASML analysis; * EUV exposures are 0.33NA equivalents, which can also include 0.55NA exposures at a ratio of one 0.55NA exposure to two 0.33NA exposures 2025 2030 19-21 25-30 DRAM: Average # of Total EUV Exposures* EUV litho spending CAGR (2025-2030): 15-25% 2025 2030 5 7-10 4-6Expected average High NA (0.55NA) Exposures 2-3Expected average High NA (0.55NA) Exposures Â Public Market share assumptions: EUV 100%, ArF immersion 90%, Dry 65% Model assumptions 2030 Page 14 Advanced Logic (â‰¤ 7nm) DRAM NAND Market Low - High Transistor CAGR (2025-2030): â€¢ Low: 28% â€¢ High: 36% Bit CAGR (2025-2030): â€¢ Low: 18% â€¢ High: 26% Bit CAGR (2025-2030): â€¢ Low: 22% â€¢ High: 30% Technology Low - High â€¢ Blend of high performance and low power designs â€¢ EUV High NA high volume from 2026 â€¢ 25-30 EUV exposures* (of which 4-6 High NA) â€¢ Blend of 4F2 and 6F2 designs â€¢ EUV High NA volume from 2026/2027 â€¢ 7-10 EUV exposures* (of which 2-3 High NA) â€¢ 3D NAND: stack of stacks & CMOS bonded array Litho Spending Low â€" High â€¢ EUV litho spending CAGR (2025-2030): 10-20% â€¢ EUV litho spending CAGR (2025-2030): 15-25% November 14, 2024 Source: ASML analysis; * EUV exposures are 0.33NA equivalents, which can also include 0.55NA exposures at a ratio of one 0.55NA exposure to two 0.33NA exposures Â Public Installed Base Management* growing installed base provides opportunity for double digit growth in service and upgrades â€¢ Growing installed base population â€¢ Service: move to value-based services â€¢ Upgrades: design for extendibility, enabling performance upgrades in the field Page 15 * Installed Base Management equals our net service and field option sales ~14% CAGR 3.7Bâ‚¬ ~6.2Bâ‚¬ 11-13Bâ‚¬ Guidance range area ~13% CAGR 2020 2024 2030 Growth drivers: Installed Base Management: services and upgrades November 14, 2024 Â Public We still model a total sales opportunity between 44Bâ‚¬ and 60Bâ‚¬ by 2030 Total sales opportunity (in â‚¬bn) Page 16 * M&I : Metrology & Inspection ** Installed Base Management equals our net service and field option sales High scenario EUV sales 32 32 Non-EUV sales (Litho and M&I*) 15 15 Installed Base Management** 13 13 Total 60 60 Moderate scenario EUV sales 26 Non-EUV sales (Litho and M&I*) 14 Installed Base Management** 12 Total 52 Low scenario EUV sales 22 22 Non-EUV sales (Litho and M&I*) 11 11 Installed Base Management** 11 11 Total 44 44 CMD 2024 Sales 2030 Not reported in CMD 2022 Logic: Compared with CMD 2022, we expect â€¢ Advanced nodes wafer demand modestly higher, offset by shift in node timing â€¢ Strategic tailwind, in particular foundry competition, lower â€¢ Mainstream nodes wafer demand slightly lower Memory: Compared with CMD 2022, we expect â€¢ DRAM wafer demand higher, driven by HPC/AI â€¢ Shift from multiple to single patterning EUV (0.33 NA and 0.55 NA) â€¢ NAND wafer demand lower Combined, these drivers result in a similar sales outlook as we have shown in CMD 2022, with a range of 44Bâ‚¬ - 60Bâ‚¬ CMD 2022 Sales 2030 Key drivers for our 2030 sales opportunity are: November 14, 2024 Â Public Gross margin development potential FY25 â€" FY30 Page 17 â€¢ EUV: volume growth and increased productivity in 0.33 NA systems positively impacting the overall GM. The volume growth in the 0.55 NA systems has a small dilutive effect on the overall GM â€¢ Non-EUV: GM increase is predominantly driven by the increase in volume. This positive GM impact is partly offset by a change in product mix (more DUV dry systems). â€¢ IBM*: GM increase due to growth in installed base and move towards more value- based services and upgrades * IBM = Installed Base Management, equals our net service and field option business Margin growth drivers ASML 2025 â€" 2030 Gross margin bridge (mid-point to mid-point guidance) ~58% 2030 Gross margin % ~52% 2025 Gross margin % FY30 GM%IBM*Non-EUVEUVFY25 GM% 2025-2030 GM% development ~4% ~1% ~1% November 14, 2024 Â Public ASML updated financial model 2030 Rounding differences may occur as these numbers / percentages are rounded to 1 decimal * Installed Base Management equals our net service and field option sales ** Cash Conversion Cycle is the sum of: accounts receivable, finance receivables, contract liabilities (including customer down payments); all divided by total net sales * 365 days. Accounts payable, inventories and vendor advance payments; all divided by total cost of sales * 365 days. *** Estimated Effective Tax Rate is based on 2024 tax legislation, and currently expected changes Latest estimate CMD 2022 Low - High market CMD 2024 Low - High market 2024 2030 2030 Total sales 28.0â‚¬bn ~44 â€" 60â‚¬bn ~44 â€" 60â‚¬bn Installed Base Management* 6.2â‚¬bn ~11 â€" 13â‚¬bn ~11 â€" 13â‚¬bn System sales 21.8â‚¬bn ~33 â€" 47â‚¬bn ~33 â€" 47â‚¬bn Gross margin ~50.6% ~56% â€" 60% ~56% â€" 60% R&D 4.3â‚¬bn (15%) ~6.0 â€" 6.6â‚¬bn ~6.0 â€" 6.6â‚¬bn SG&A 1.1â‚¬bn (4%) ~1.6â‚¬bn ~1.7 â€" 1.9â‚¬bn Capex 1.9â‚¬bn (7%) ~1.5â‚¬bn ~2.5â‚¬bn Cash Conversion Cycle** <200 days <200 days <200 days Effective Tax Rate*** 16-17% ~16.5% ~17% November 14, 2024 Page 18 Â Public November 14, 2024 Page 19 Flexible workforce Employees Additional flexibility through the hour bank and other measures D&E Fix labor and other costs D&E Flex labor and farm-out Own personnel Flex workers Outsourced R&D R&D spend Systems Cost of Goods (COG) at Standard, composition Majority of systems COG is externally sourced 95% 5% 2023 78% 22% 2023 13% 87% 2023 We are and remain flexible in our operating model to deal with the industry volatility and uncertainties Labor Materials Â Public November 14, 2024 Page 20 Historical shareholder value creation Continuing growth Continued shareholder value creation Page 20 Â Public Page 21 Our approach to capital allocation and financing Focused investment in our business supported by a strong and flexible balance sheet Capital allocation â€¢ Investments to execute ASMLâ€™s long term roadmap â€¢ Cash returns to shareholders â€¢ Sustainable dividend per share that will grow over time, paid quarterly â€¢ Return excess cash to shareholders through share buybacks Financing â€¢ Maintain sufficient liquidity to ensure continued business growth and to provide buffer for cash flow volatility â€¢ Maintain a capital structure that targets a solid investment-grade credit rating November 14, 2024 Â Public Page 22 Our approach to capital allocation Continued shareholder value creation R&D Capex Cumulative share buyback Cumulative dividend *ASML contribution for Zeiss SMT capex included as of 2017 ** 2024E is estimate for the FY2024 figures Focused investment in our business through R&D, Capex Cash returns to shareholders 2014 2015 2016 2017* 2018 2019 2020 2021 2022 2023 2024E** 1,1 1,1 1,1 1,3 1,6 2,0 2,2 2,5 3,3 4,0 4,3 0,4 0,4 0,3 0,4 0,6 0,9 1,0 0,9 1,3 2,2 1,9 1,4 1,4 1,4 1,6 2,2 2,9 3,2 3,5 4,6 6,2 6,2 4,4 4,9 5,3 5,8 7,0 7,4 8,6 17,2 21,8 22,8 23,3 1,1 1,4 1,9 2,4 3,0 4,3 5,4 6,7 9,3 11,1 13,5 5,5 6,4 7,2 8,2 10,0 11,7 14,0 23,9 31,1 33,9 36,8 up to 2014 2015 2016 2017 2018 2019 2020 2021 2022 2023 2024E** HMI acquisition (â‚¬2.8bn) Carl Zeiss SMT Holding acquisition 24.9% interest (â‚¬1.0bn) Berliner Glas acquisition (â‚¬0.3bn) [â‚¬ b n] [â‚¬ b n] We expect to continue to return significant amounts of cash to our shareholders through a combination of growing dividends and share buybacks November 14, 2024 Â Public Business model and capital allocation strategy Our continued investments in technology leadership have created significant shareholder value. Investments create value We expect substantial growth opportunities in this decade Based on different market and technology scenarios, we see an opportunity to achieve the following by 2030: â€¢ Annual revenue between approximately â‚¬44 billion and â‚¬60 billion with gross margin between approximately 56% and 60% Market and technology opportunity Expected growth in semiconductor end markets and increasing lithography spending on future nodes fuel demand for our products and services. Growth in markets We confirm our financing policy; a solid capital and liquidity structure, based on which we will continue to invest in our business and expect to return significant amounts of cash to our shareholders through growing dividends and share buybacks. Capital allocation and financing Key messages Page 23 Â Public Forward Looking Statements This document and related discussions contain statements that are forward-looking within the meaning of the U.S. Private Securities Litigation Reform Act of 1995, including statements with respect to our strategy, plans and expected trends, including trends in end markets and the technology industry and business environment trends, including the emergence of AI and its potential opportunities and expectations for the semiconductor industry, including computing power, advanced logic nodes and DRAM memory, statements with respect to Mooreâ€™s law and expected transistor growth and aspirations by 2030, global market trends and technology, product and customer roadmaps, long term outlook and expected lithography and semiconductor industry growth and trends and expected growth in semiconductor sales and semiconductor market opportunity through to 2030 and beyond, expected growth in wafer demand and capacity and additional wafer capacity requirements, expected investments by our customers, including investments in our technology and in wafer capacity, plans to increase capacity, expected growth in lithography spend, growth opportunities including opportunities for growth in service and upgrades and opportunities for growth in Installed Base Management sales, expected growth and gross margins in the holistic lithography business and expected addressable market for Applications products, expectations and benefits of a growing installed base, ASMLâ€™s and its supplierâ€™s capacity, expected production of systems, model scenarios and the updated model for 2030, including annual revenue and gross margin opportunity and development potential for 2030, outlook and expected, modelled or potential financial results, including revenue opportunity, gross margin, R&D costs, SG&A costs, capital expenditure, cash conversion cycle and annualized effective tax rate for 2030 and assumptions and drivers underlying such expected, modelled or potential amounts, and other assumptions underlying our business and financial models, expected trends, outlook and growth in semiconductor end markets and long term growth opportunities, demand and demand drivers, expected opportunities and growth drivers for and technological innovation of our products including DUV EUV, High NA, Hyper NA, Applications, and other products impacting productivity and costs, transistor dimensions, logic and DRAM shrink, foundry competition, statements with respect to dividends and share buybacks and our capital return policy, including expectation to return significant amounts of cash to shareholders through growing dividends and buybacks and statements with respect to energy generation and consumption trends and the drive toward energy efficiency, emissions reduction and greenhouse gas neutrality goals and target dates to achieve greenhouse gas neutrality, zero waste from operations and other ESG targets and ambitions and plans to maintain a leadership position in ESG, increasing technological sovereignty across the world and the expected impact on semiconductor sales, including specific goals of countries across the world, increasing competition in the foundry business, estimates for 2024 and other non-historical statements. You can generally identify these statements by the use of words like "may", "will", "could", "should", "project", "believe", "anticipate", "expect", "plan", "estimate", "forecast", "potential", â€œopportunityâ€, â€œscenarioâ€, â€œguidance,â€ "intend", "continue", "target", "future", "progress", "goal" and variations of these words or comparable words. These statements are not historical facts, but rather are based on current expectations, estimates, assumptions, models, opportunities and projections about our business and our future and potential financial results and readers should not place undue reliance on them. Forward- looking statements do not guarantee future performance and involve a number of substantial known and unknown risks and uncertainties. These risks and uncertainties include, without limitation, customer demand, semiconductor equipment industry capacity, worldwide demand for semiconductors and semiconductor manufacturing capacity, lithography tool utilization and semiconductor inventory levels, general trends and consumer confidence in the semiconductor industry and end markets, the impact of general economic conditions, including the impact of the current macroeconomic environment on the semiconductor industry, uncertainty around a market recovery including the timing thereof, the impact of inflation, interest rates, wars and geopolitical developments, the impact of pandemics, the performance of our systems, the success of technology advances and the pace of new product development and customer acceptance of and demand for new products, our production capacity and ability to adjust capacity to meet demand, supply chain capacity, timely availability of parts and components, raw materials, critical manufacturing equipment and qualified employees, our ability to produce systems to meet demand, the number and timing of systems ordered, shipped and recognized in revenue, risks relating to fluctuations in net bookings and our ability to convert bookings into sales, the risk of order cancellation or push outs and restrictions on shipments of ordered systems under export controls, risks relating to technology, product and customer roadmaps and Mooreâ€™s law, risks relating to the trade environment, import/export and national security regulations and orders and their impact on us, including the impact of changes in export regulations and the impact of such regulations on our ability to obtain necessary licenses and to sell our systems and provide services to certain customers, exchange rate fluctuations, changes in tax rates, available liquidity and free cash flow and liquidity requirements, our ability to refinance our indebtedness, available cash and distributable reserves for, and other factors impacting, dividend payments and share repurchases, the number of shares that we repurchase under our share repurchase programs, our ability to enforce patents and protect intellectual property rights and the outcome of intellectual property disputes and litigation, our ability to meet ESG goals and execute our ESG strategy, other factors that may impact ASMLâ€™s business or financial results including the risk that actual results may differ materially from the models, potential and opportunity we present for 2030 and other future periods, and other risks indicated in the risk factors included in ASMLâ€™s Annual Report on Form 20-F for the year ended December 31, 2023 and other filings with and submissions to the US Securities and Exchange Commission. These forward-looking statements are made only as of the date of this document. We undertake no obligation to update any forward-looking statements after the date of this report or to conform such statements to actual results or revised expectations, except as required by law. This document and related discussions contain statements relating to our approach to and interim progress on achieving certain energy efficiency and greenhouse gas emissions reduction targets, including our ambition to achieve greenhouse gas neutrality. References to â€œgreenhouse gas neutralâ€ means remaining emissions, after ASMLâ€™s efforts to reach its GHG emission reduction targets, compensated by the same amount of metric tons of carbon credits that are verified against recognised quality standards. Page 24November 14, 2024 Â Public November 14, 2024 Page 25 THANK YOU Â EX-99.8 9 exhibit998.htm EX-99.8 exhibit998 Public Christophe Fouquet Closing remarks ASML Investor Day Veldhoven, The Netherlands November 14, 2024 President and Chief Executive Officer Small Talk 2024 Exhibit 99.8 Â Public â€¢ The Semiconductor Industry remains strong and Artificial Intelligence is expected to create further opportunity as major investments in supercomputing are happening and the entire industry is preparing to insert AI in all critical future applications â€¢ Our industry will require major innovations to address the anticipated cost and power consumption challenges of AI and this will further boost the industry roadmap in a product mix shifting towards advanced logic and DRAM â€¢ Our customers remain at the core of our strategy, and we believe that lithography will remain at the heart of their innovation. We also anticipate that an increased number of critical lithography exposures for advanced logic and memory processes will continue to support our customers in addressing their challenges â€¢ We expect that our ability to 1) scale our EUV technology well into the next decade, 2) extend holistic lithography into supporting 3D front end integration and 3) improve the performance and cost effectiveness of our DUV products will continue to address all our customers needs with a flexible and versatile portfolio â€¢ We will continue to leverage our large and growing systems installed base (DUV, EUV) to provide high value service and upgrades over a >20 years lifetime â€¢ ASML values the strong industry partnerships which are critical to our success and our collective commitment to a leadership position in ESG We expect that our ability to scale EUV technology into the next decade and extend our versatile holistic lithography portfolio could place ASML at the heart of the AI opportunity. This would continue to create significant growth in revenue and profitability in this decade. November 14, 2024 Page 2 Â Public â€¢ The long-term outlook for the semiconductor industry remains promising, given the role of semis as mission-critical enablers of multiple megatrends. As a result, we expect global semi sales to grow at 9% CAGR (2025-2030) & surpass $1T by 2030. â€¢ This translates into an overall wafer demand growth of 780K wafer starts per month per year (2025-2030). â€¢ The rise of AI as a leading end driver also implies a positive mix-shift in the wafer demand profile from litho spending perspective. â€¢ We expect 5-8% extra overall wafer capacity by 2030 on top of demand-driven additions, owing to strategic considerations. â€¢ We expect Advanced Logic & DRAM shrink to drive further EUV litho layers & spending. â€¢ For Advanced Logic, we expect an EUV litho spending CAGR of 10-20%. â€¢ For DRAM, we expect an EUV litho spending CAGR of 15-25%. â€¢ This expected growth in semiconductor end markets and increasing lithography spending on future nodes fuel demand for our products and services â€¢ Based on different market and lithography intensity scenarios, we see an opportunity to achieve 2030 annual revenue between approximately â‚¬44 billion and â‚¬60 billion with gross margin between approximately 56% and 60% â€¢ We expect to continue to return significant amounts of cash to our shareholders through a combination of growing dividends and share buybacks Industry dynamics continue to create opportunity for significant growth in revenue and profitability in this decade November 14, 2024 Page 3 Â Public Forward Looking Statements This document and related discussions contain statements that are forward-looking within the meaning of the U.S. Private Securities Litigation Reform Act of 1995, including statements with respect to our strategy, plans and expected trends, including trends in end markets and the technology industry and business environment trends, including the emergence of AI and its potential opportunities and expectations for the semiconductor industry, including computing power, advanced logic nodes and DRAM memory, statements with respect to Mooreâ€™s law and expected transistor growth and aspirations by 2030, global market trends and technology, product and customer roadmaps, long term outlook and expected lithography and semiconductor industry growth and trends and expected growth in semiconductor sales and semiconductor market opportunity through to 2030 and beyond, expected growth in wafer demand and capacity and additional wafer capacity requirements, expected investments by our customers, including investments in our technology and in wafer capacity, plans to increase capacity, expected growth in lithography spend, growth opportunities including opportunities for growth in service and upgrades and opportunities for growth in Installed Base Management sales, expected growth and gross margins in the holistic lithography business and expected addressable market for Applications products, expectations and benefits of a growing installed base, ASMLâ€™s and its supplierâ€™s capacity, expected production of systems, model scenarios and the updated model for 2030, including annual revenue and gross margin opportunity and development potential for 2030, outlook and expected, modelled or potential financial results, including revenue opportunity, gross margin, R&D costs, SG&A costs, capital expenditure, cash conversion cycle and annualized effective tax rate for 2030 and assumptions and drivers underlying such expected, modelled or potential amounts, and other assumptions underlying our business and financial models, expected trends, outlook and growth in semiconductor end markets and long term growth opportunities, demand and demand drivers, expected opportunities and growth drivers for and technological innovation of our products including DUV EUV, High NA, Hyper NA, Applications, and other products impacting productivity and costs, transistor dimensions, logic and DRAM shrink, foundry competition, statements with respect to dividends and share buybacks and our capital return policy, including expectation to return significant amounts of cash to shareholders through growing dividends and buybacks and statements with respect to energy generation and consumption trends and the drive toward energy efficiency, emissions reduction and greenhouse gas neutrality goals and target dates to achieve greenhouse gas neutrality, zero waste from operations and other ESG targets and ambitions and plans to maintain a leadership position in ESG, increasing technological sovereignty across the world and the expected impact on semiconductor sales, including specific goals of countries across the world, increasing competition in the foundry business, estimates for 2024 and other non-historical statements. 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